MPSoC'26

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Beyond Moore's Law: Driving Competitive Advantage with 3D-Stacked Multi-Die Systems

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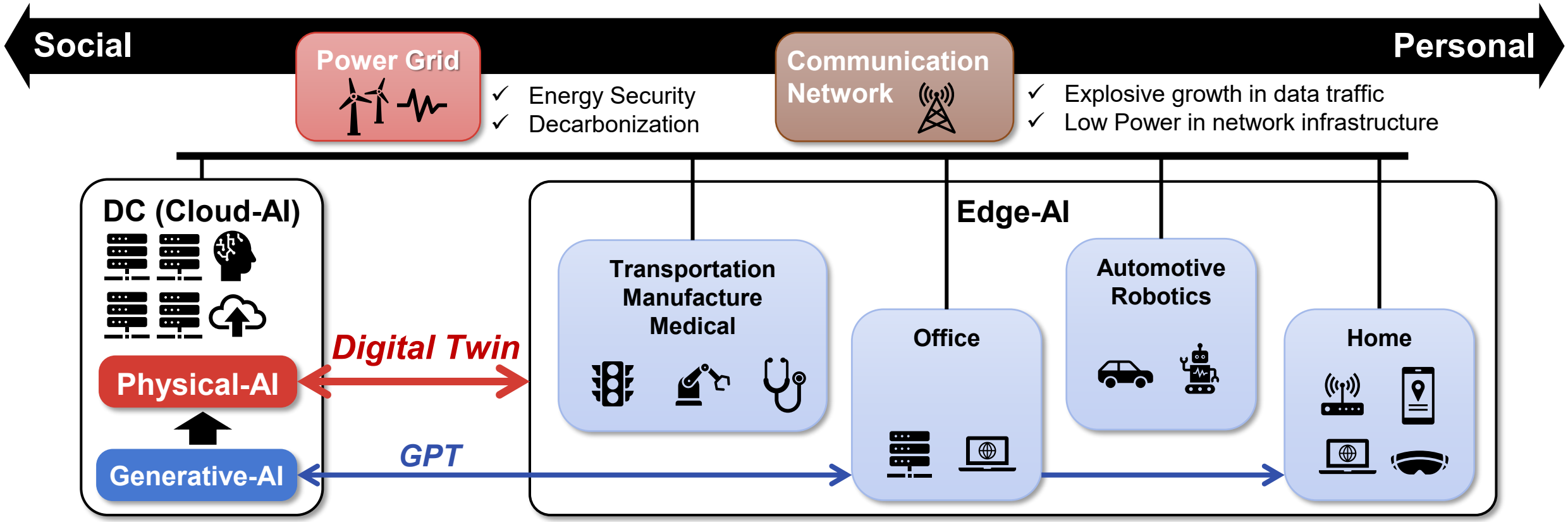
June 23rd , 2026

What to expect in this presentation?

- Shift beyond monolithic SoCs
  → why 3DIC/advanced packaging matters
- Overview of TSMC SoIC® and chiplet architectures
- End-to-end multi-die design flow
  (architecture → signoff)
- Key challenges: power, thermal, connectivity, test
- Solutions: unified 3DIC flow, EDA, IP integration
- Real-world case study: 2 dies taped out in 7 months

Smart Society Change from Generative-AI to Physical-AI

AI systems that gather data from the real world and act in the real world. Significantly greater computation and data transfer are required, on the Cloud and on the Edge.



- ✓ High Performance (High Integrated)
- ✓ Huge memory capacity, huge memory transaction
- ✓ Low Power (Cooling Cost)
- ✓ High Reliability, Security

- ✓ High Performance
- ✓ Small / Thin Factor
- ✓ Low Power (Low Bill, Battery backup)

- ✓ Low latency, guaranteed performance
- ✓ High Reliability (Automotive, Robotics)
- ✓ Security (Company / Personal data protection)

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Chiplets Enabling Scalable System-Level Collaborative Design

Fundamental Challenges

- **Limits of Moore's Law** — The slowdown of logic process evolution.
- **Architecture** — Shift from CPU centric to parallel specialized architectures GPUs, TPUs, NPUs.
- **Memory Wall** — Memory BW evolution is slower than Logic performance evolution.

Breaking Through the Limits of Moore's Law

- **Homogeneous Chiplets**
  - High-density integration beyond the reticle limit.
  - Yield optimization through die partitioning in advanced process nodes.
  - Sharing DRAM across multiple dies via a cache-coherent bus architecture.

Intelligent System Partitioning and Advanced Integration

- **Heterogeneous Chiplets**
  - Integration of large-scale logic and high-bandwidth memory against the Memory Wall.
  - Integration of heterogeneous logic technologies.
  - Chiplet reuse and replacement.

Multi-Die Design Challenges

Design optimization across chiplet, advanced packages (interposer/substrate), balancing reliability, thermal behavior, PI/SI, memory and interconnects

Monolithic SoC

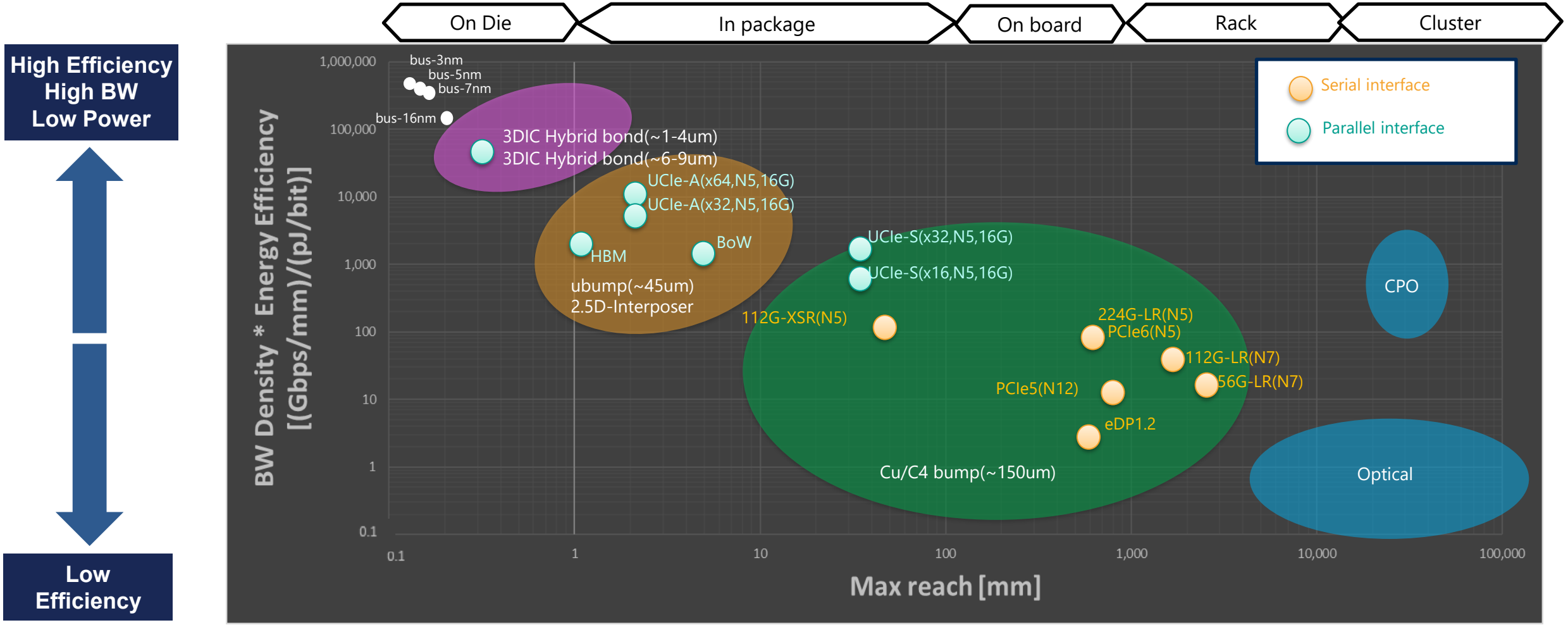
Chiplet Challenges

- System partitioning
- Standardised die-to-die & chip-to-chip connectivity
- Standardised hierarchical test and repair
- Power, signal integrity & thermal management
- Design flow - System Verification
- System signoff analysis

Multi-Die Design

Bit Delivery Efficiency

Dedicated D2D I/F IP and Advanced Packaging enable system portioning across multi-die without power the power, latency and density penalty olf traditional packaging



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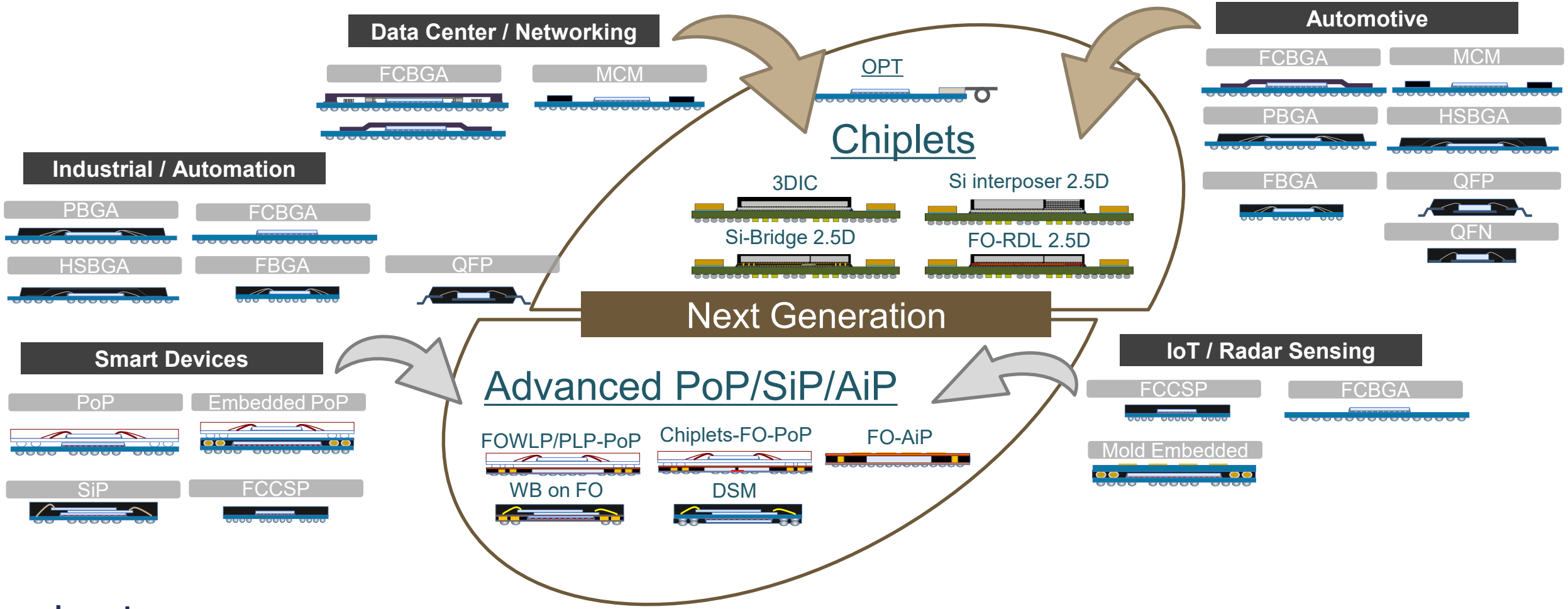
Package Roadmap

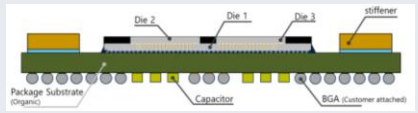
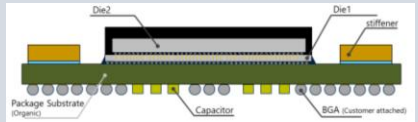
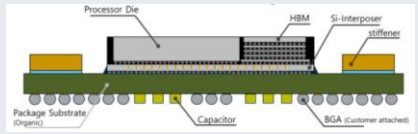
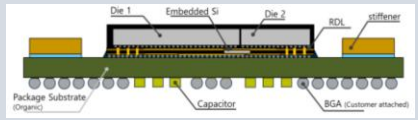
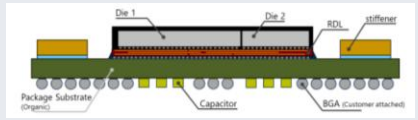
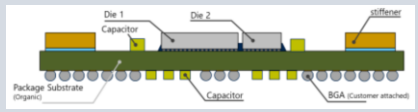
Packaging has become a core innovation layer enabling AI, chiplets and system-level scaling beyond Moore's Law.



Intro into Advanced Packages

Higher-density 3D hybrid bonding enables far greater interconnect density and scaling, while 2D packaging types trade off density for simpler integration

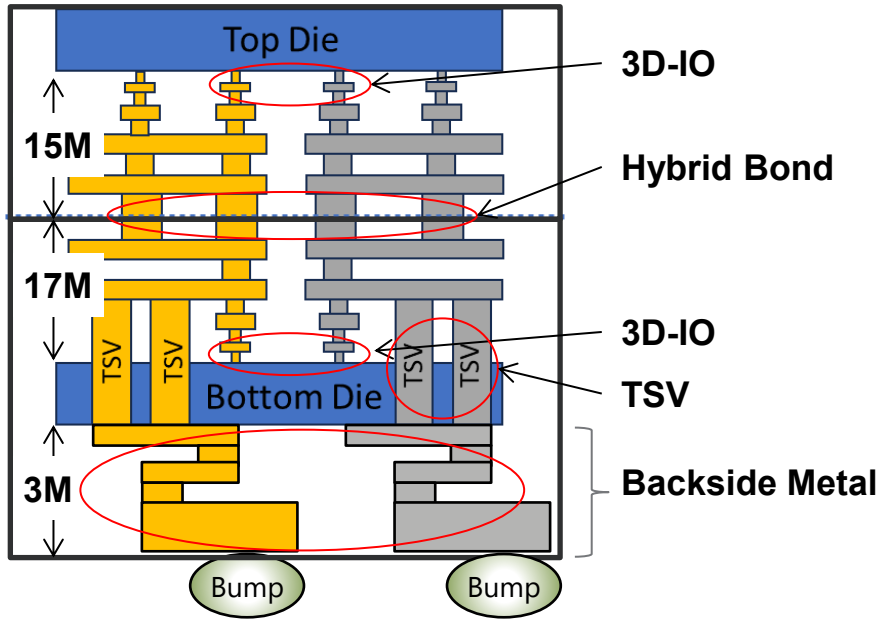
Design TAT, Cost

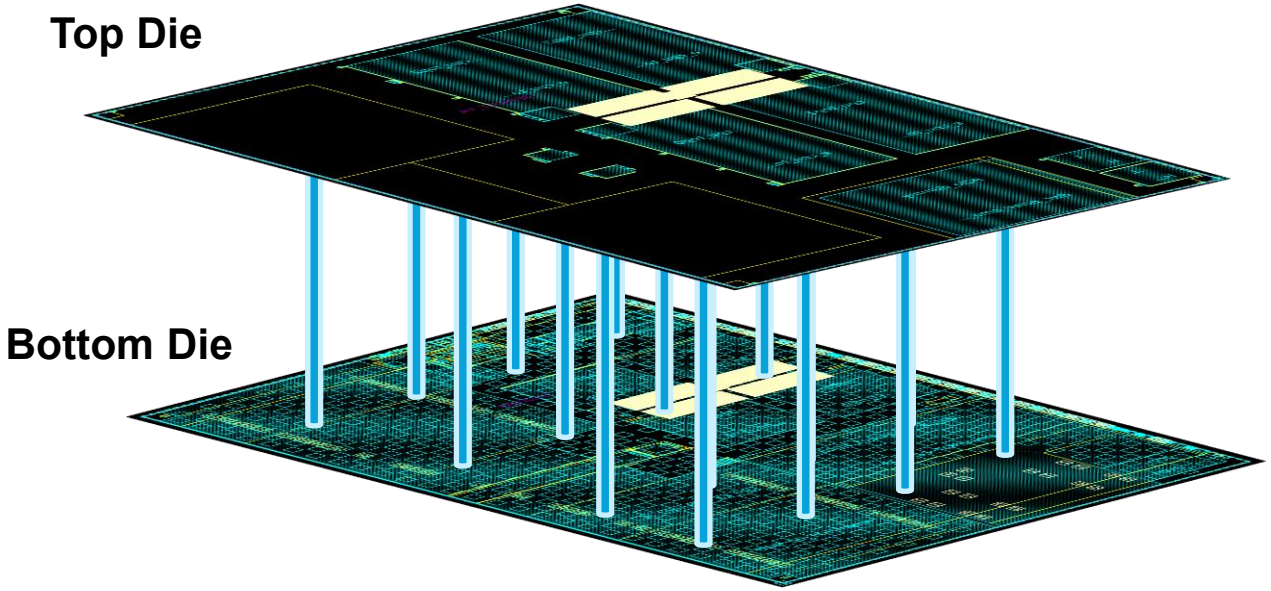
D2D Connect Technologies	Structure	D2D Min. Bump Pitch [μm] Normal (Enhanced)	No. of lanes per layer [/mm] Normal (Enhanced)	Data rate per lane
3D (hybrid bonding)		9(6)	1.2*10E4(2.8*10E4) [/mm2]	~5Gbps
3D (u-bump)		40(20)	676(2601) [/mm2]	~5Gbps
Si-Interposer/CoWoS-S		55(40)	10^3	~16Gbps
Si-Bridge		55(45)	10^3	~16Gbps
FO-RDL/CoWoS-R		55(45)	10^2	~16Gbps
MCM		150(130)	10^1	~112Gbps

Structure of 3DIC

Top Die	**Technology Nodes**	**TSMC N3P/ 1P15M**
	Size	**19.80mm2**
Bottom Die	**Technology Nodes**	**TSMC N5/ 1P17M**
	Size	**21.8mm2**

3D-IC Chip





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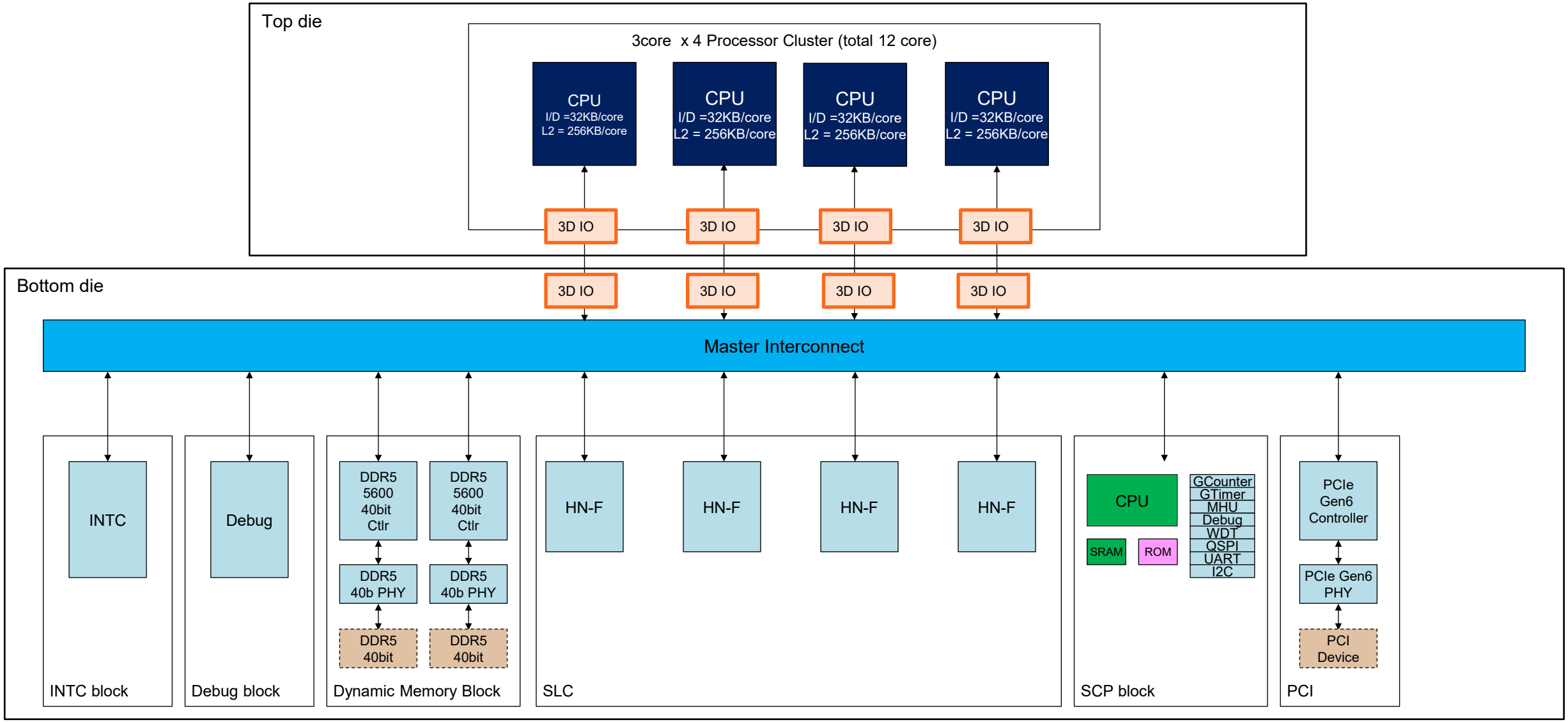
Design

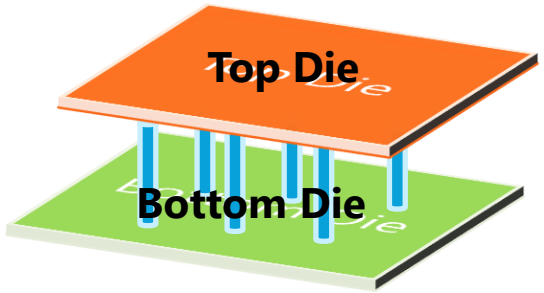
3DIC Test Chip Electrical Architecture – Logic on Logic

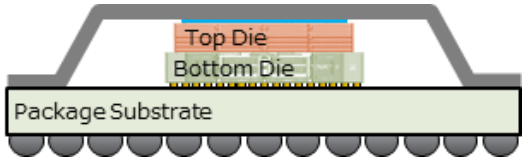


Chip Specification

Logic-on-Logic 3DIC with TSMC-SoIC®

Items	Specification	Description
3D-IC Technology	TSMC-SoIC®	Face to Face Structure
Top Die (Compute)	Technology Nodes	N3P / 1P15M
	Size	19.80mm2
	CPU	3Core x4Cluster
	Hardware Sequencer	Heat Source Circuit
	Synopsys SLM IP	DTS x1, RTS x6, PD x1, VM x1, GD x8
Die-to-Die	Hybrid Bond	3DIO
Bottom Die (Interface)	Technology Nodes	N5 / 1P17M
	Size	21.8mm2
	SLC	1MB
	DDR5	80bit / 5,500Mbps
	PCIe® Gen6	4Lane
	QSPI	1ch
	UART	5ch
	I2C	4ch
	Hardware Sequencer	Heat Source Circuit
	PVT Sensor	DTS x1, RTS x5, PD x1, VM x1
Package	Type	FCBGA
	Size	25mmSQ
	Ball pitch	0.8mm

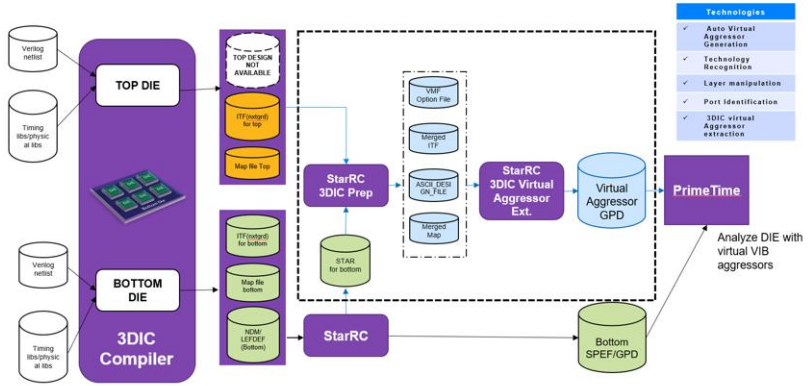


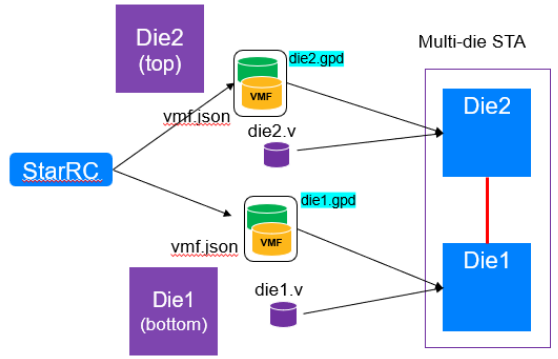


3D-IC Design Flow

Key Challenges

- **Development Schedule**
  Need to complete the design and tape-out of two dies in only seven months.
  → Require high-quality design environment and design flow for TSMC-SoIC®
- **Logic-on-Logic Structure**
  Some IPs are implemented on top die and bottom die
  → Requires IP design considering TSV and signal/dummy HB
  → Requires 3D test method
  Synchronous path between top and bottom dies must be automatically connected and signed off
  → Requires automatic D2D connection by D2D IO
  → Require LPE and STA analysis for D2D
  Difficult to supply power evenly to upper logic layers
  → Requires EMIR analysis
  High heat density due to stacked logic layers
  → Require thermal analysis
  Design for Test (DFT) Flow for 3D-IC

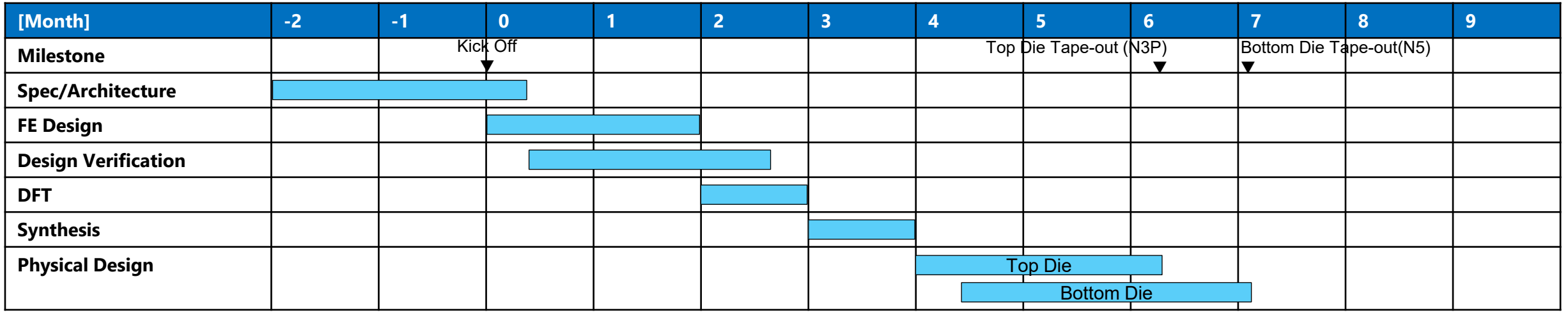




Development Schedule

Achieved tape-out of 2 Dies in 7 months from the start of design

- With Synopsys entire TSMC-SoIC® design environment
- With Synopsys Cloud environment to drive efficient development

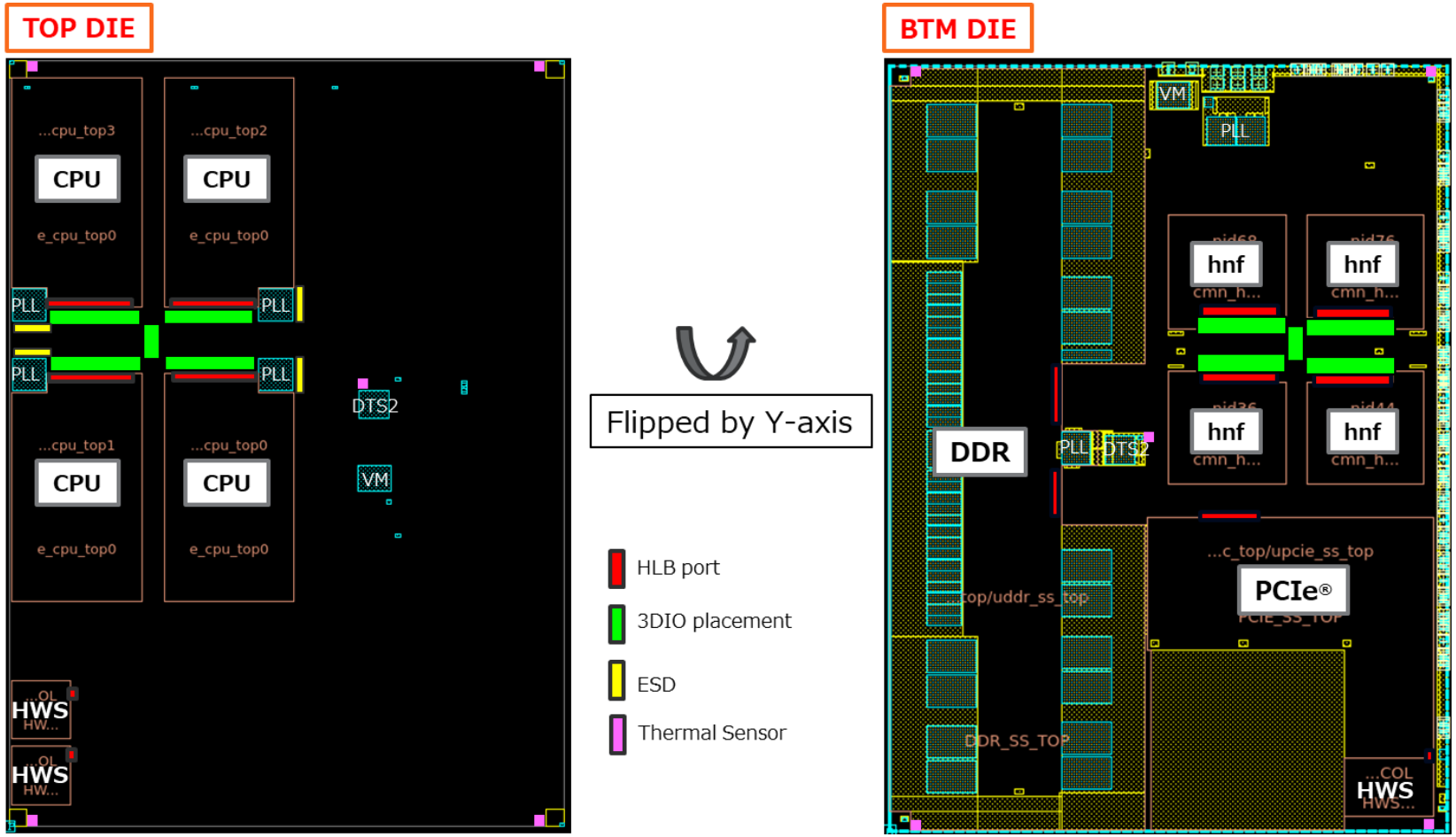


Design Phase	Contents	Synopsys Tools
Logic Synthesis	2D Synthesis	Fusion Compiler
Floor Planning	Die Stacking, TSV, Bump Placement, PG/Backside metal route	3DIC Compiler
P&R	Placement/Clock/route	Fusion Compiler
ECO	ECO	Prime Closure
Extraction & STA	3D LPE (Top, Bottom, IDX), 3D STA (Boundary Model, Virtual IDX)	StarRC, PrimeTime
Power Integrity	EM/IR analysis	Ansys Redhawk-SC
Physical verification	Interface DRC/LVS, Die DRC/LVS	IC Validator
DFT	DFT Design	TestMAX DFT

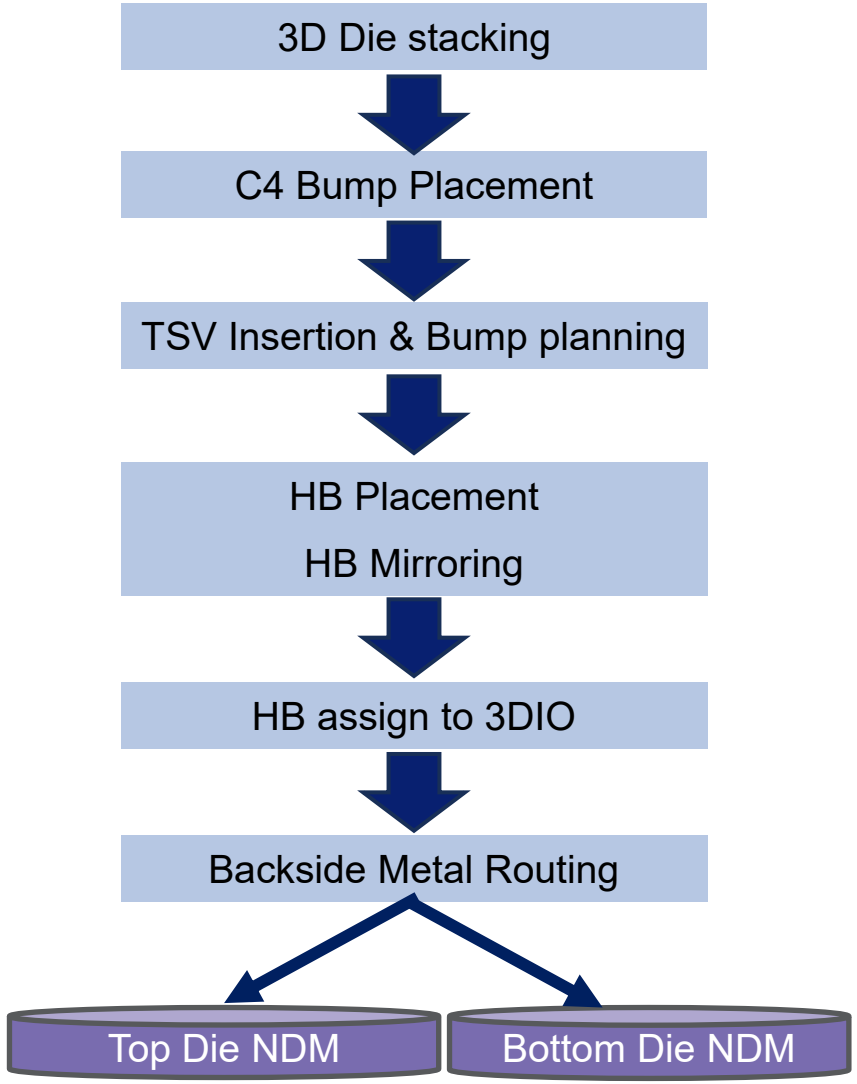
3D Heterogeneous Stack Die Floorplan

Top Die and Bottom Die Floor Plan

- DDR and PCIe® IPs are implemented on bottom Die
- PVT sensors are implemented in top die and bottom die



3D Design Planning

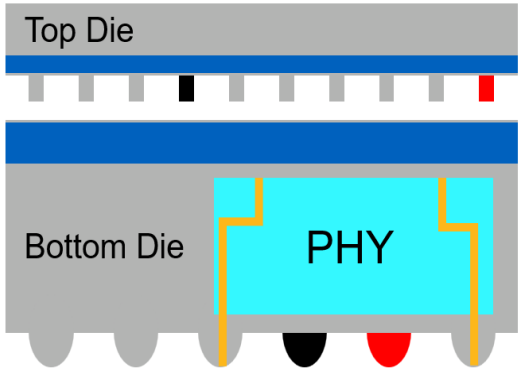


- N3 die stacked on top N5 die in F2F configuration
- C4 bump map from pkg i/o file
- TSV insertion following N5 rules
- Hybrid Bond (HB) planning (PG, Signal, Dummy)
- 3DIO signal assignment to HB
- Backside PG routing on bottom die
- Data hand-off for die implementation

3D-Enabled Synopsys IP(s) in Testchip

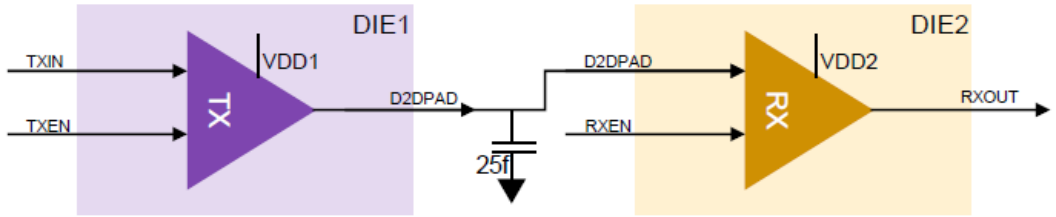
PCIe® 6.0 and DDR5 Interface IP

- Both PHYs are customized for F2F 3D configuration
- The PHYs are implemented in the bottom die
- Interface IP PHY modified from face down flip chip to face up bottom die implementation
- Power and Ground and signals re-routed from bumps through TSVs to C4



3DIO IP for 3D die-to-die connectivity

- RX-3DIO and TX-3DIO implemented in Testchip tapeout



Overcoming Die-to-Die Connectivity Challenges with Synopsys 3DIO IP

Challenges

- Find an easy way to insert 3DIO IP in P&R flow
- Need for flexible IP and tap cell placement
  - To minimize D2D path and ESD robustness
  - To solve complex tap placement rules
- Support minimum D2D signal routing
  - Smaller metal resistance
- Ability to fix antenna error

Synopsys 3DIO IP Solution

Developed with Socionext

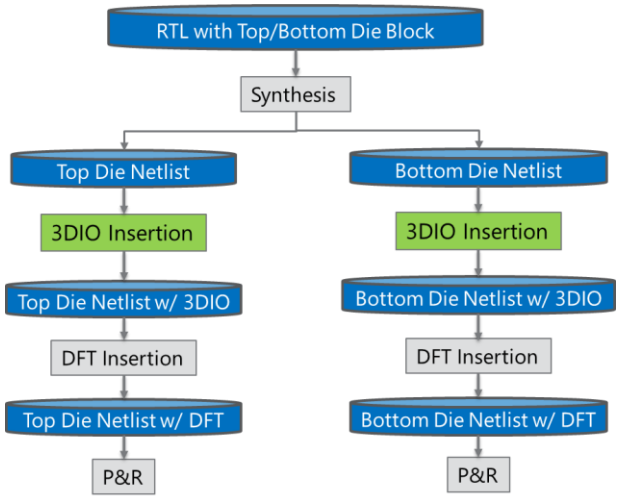
- Feature rich 3DIO library
- Wide range support for PVT
- Excellent integration with the P&R tool

Item	Synopsys 3DIO IP
Cell kind variation	BD, TX, RX, SS-3DIO, 3DIO-PHY
Support voltage	0.55V/0.65V/0.75V ±10%
Temperature	-40℃ - 125℃
Speed	up to 3GHz
IO Drive strength Variations	BD : 4, TX : 4, RX : 2
Composition	ESD(CDM), ANT, Buffer

Synopsys 3DIO IP for 3D Die-to-Die Connectivity

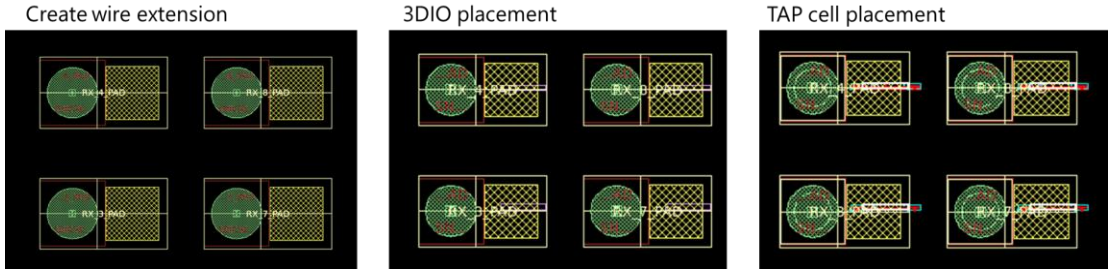
3DIO IP insertion in P&R flow

- Automatic 3DIO insertion utility available in Synopsys Fusion/3DIC Compiler
  - Insertion available in 3DIC Compiler with automatic driver/load identification
  - Auto select the RX/TX cells for insertion



3DIO IP and tap cell placement

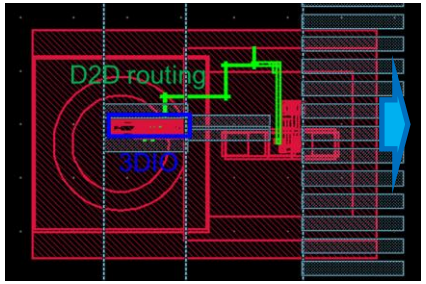
- Automatic 3DIO placement under routing violations (RV)
- Avoid TAP spacing violations
- Place abutted TAP cell for ESD protection



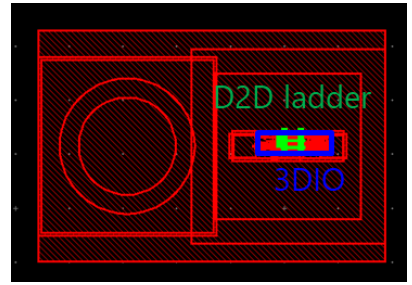
D2D signal routing

- Routing from 3DIO pin to Hybrid Bonding by ladder wire

Long routing wire from 3DIO to RV



Minimize routing wire with ladder

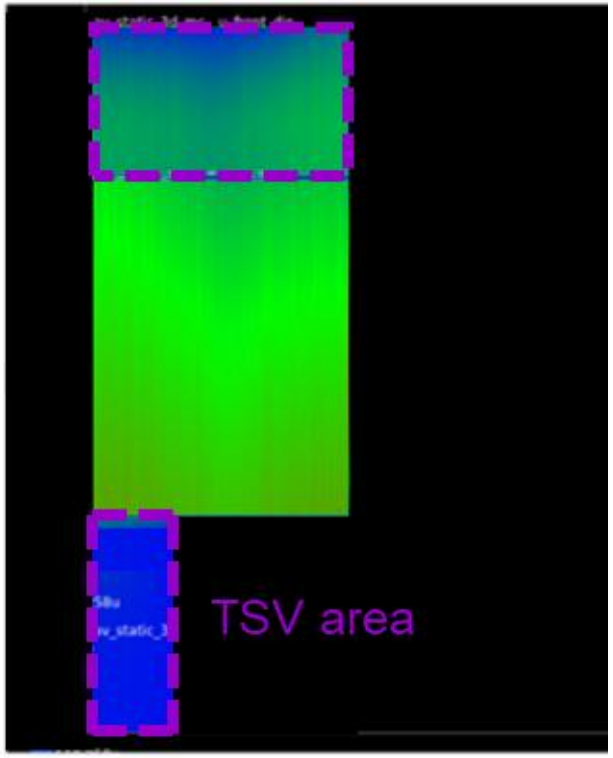


Early Rail Analysis (ERA) and IRD optimization for 3DIC

TSV Optimization through feedback of ERA results

TSV location at initial stage

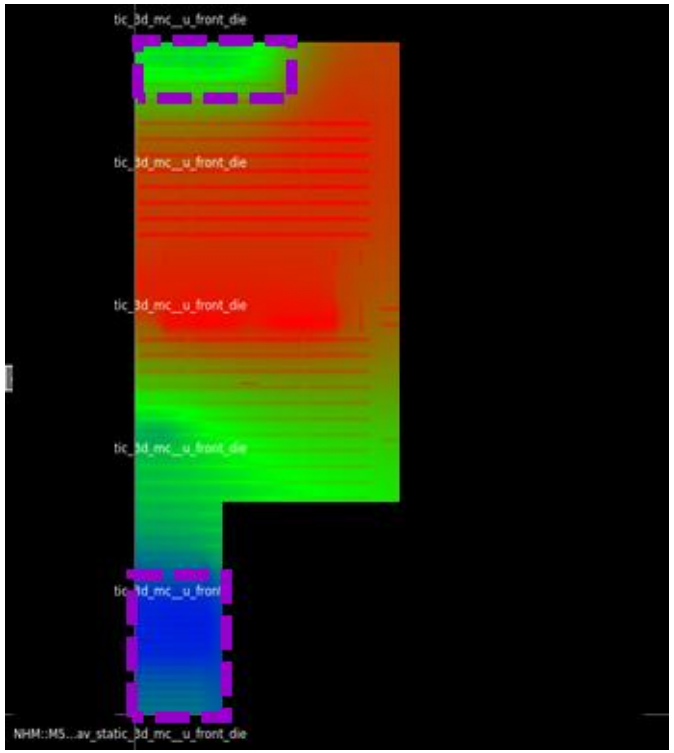
Initial ERA result
(Initial floorplan)



Annotate TSV info

TSV location is limited due to placement constraints causing, large IR Drop

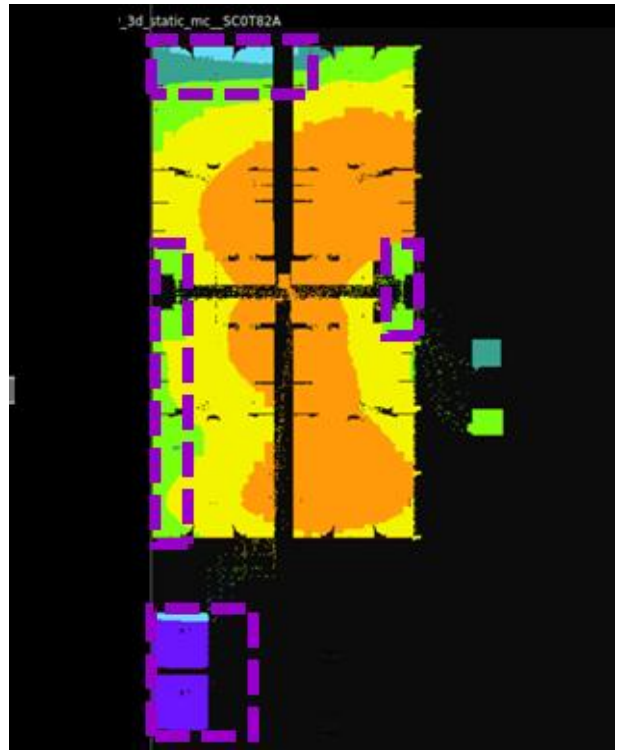
Intermediate ERA result
(Design Update)



Improve TSV location

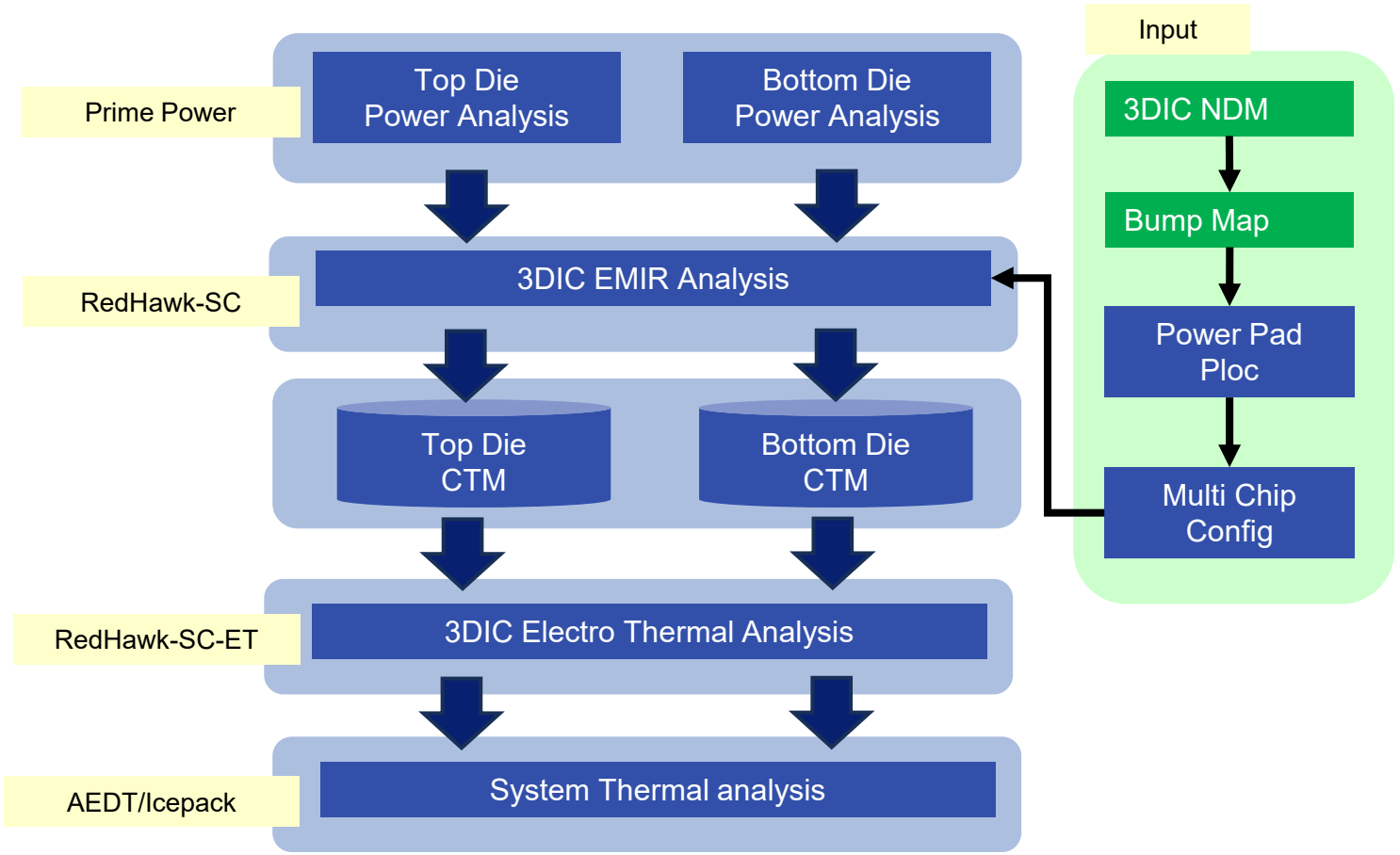
Improved IR Drop by TSV optimization through feedback from ERA results

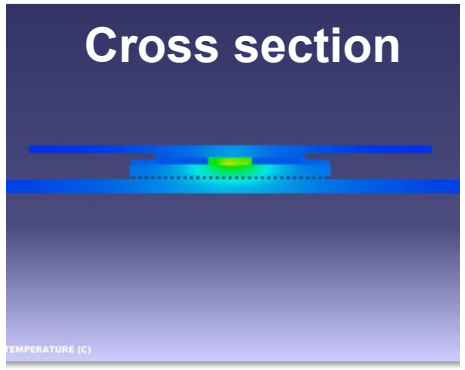
Sign off IRD results
(Final result)

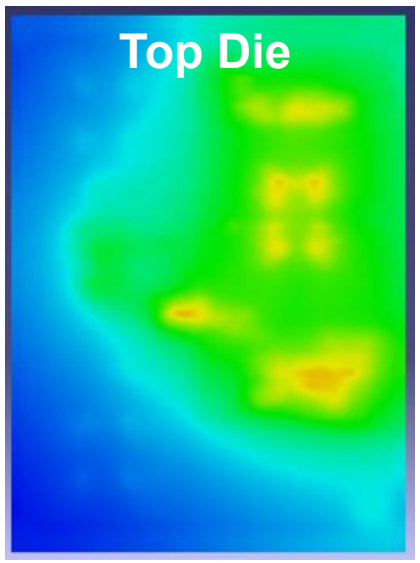


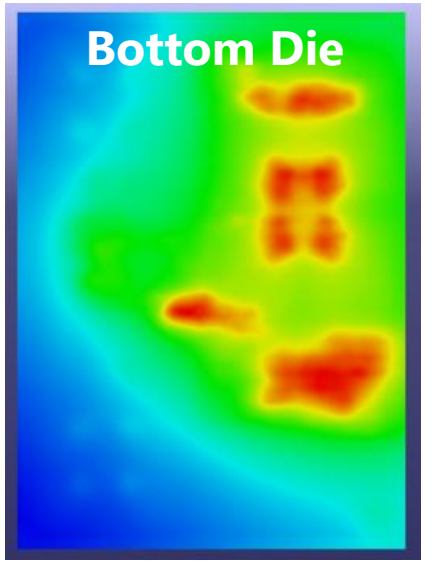
3DIC Thermal Analysis

Thermal analysis considering thermal coupling between dies







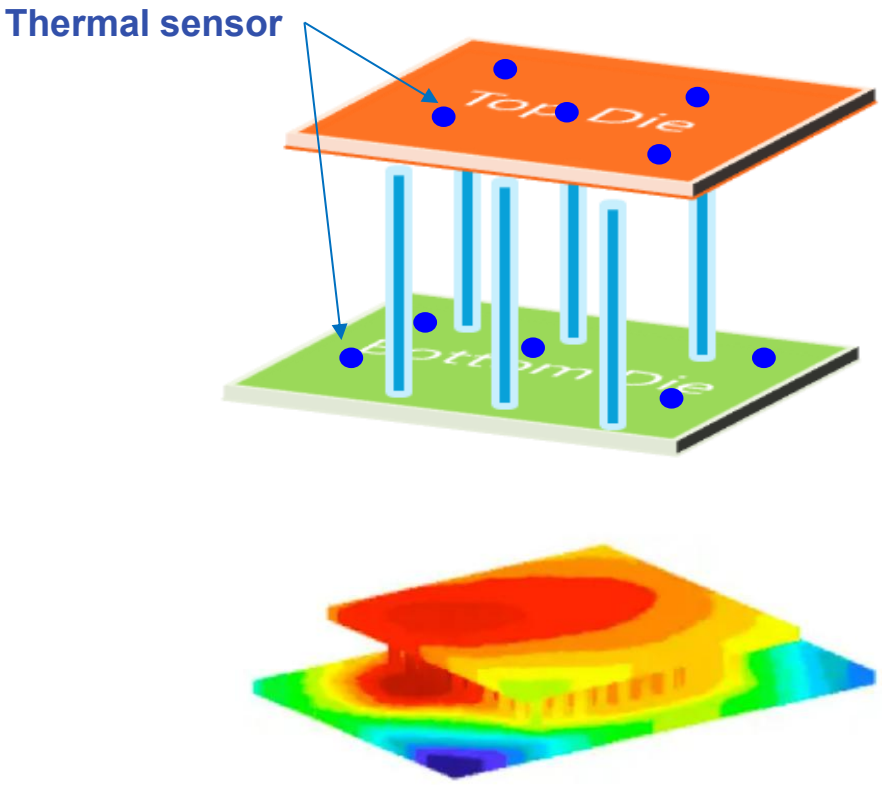


Met the criteria
include thermal conduction between dies

Thermal Evaluation and Analysis

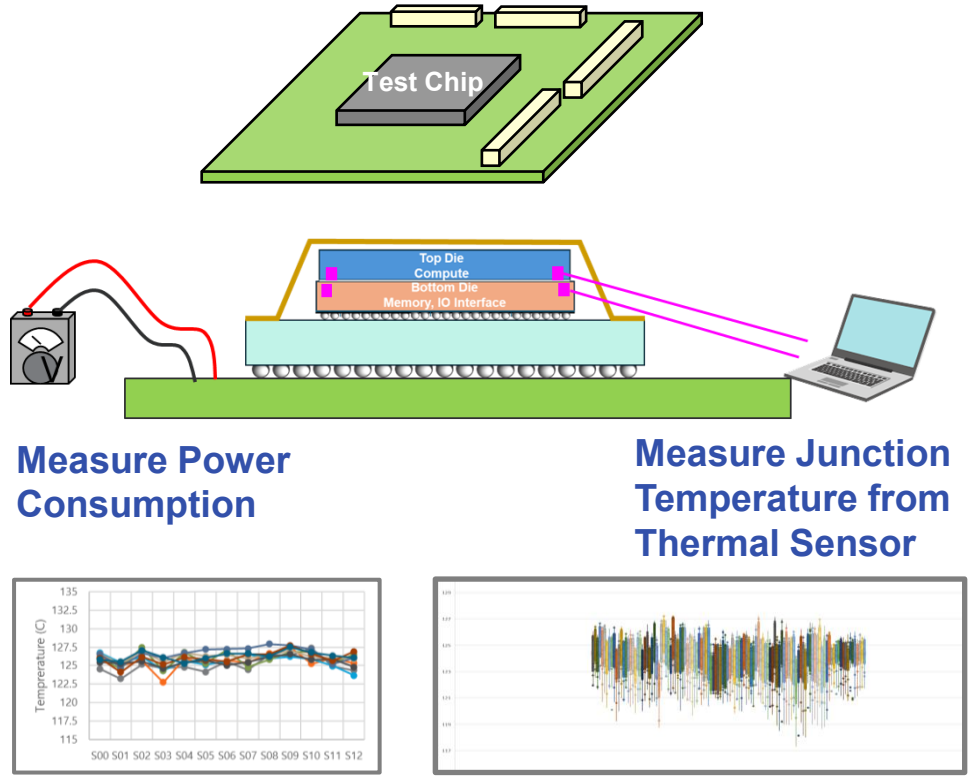
Thermal simulation and validation using test chip

- Evaluate and analyze thermal using thermal sensor
- Correlate simulation results and test chip results



Thermal Simulation Result

Correlate

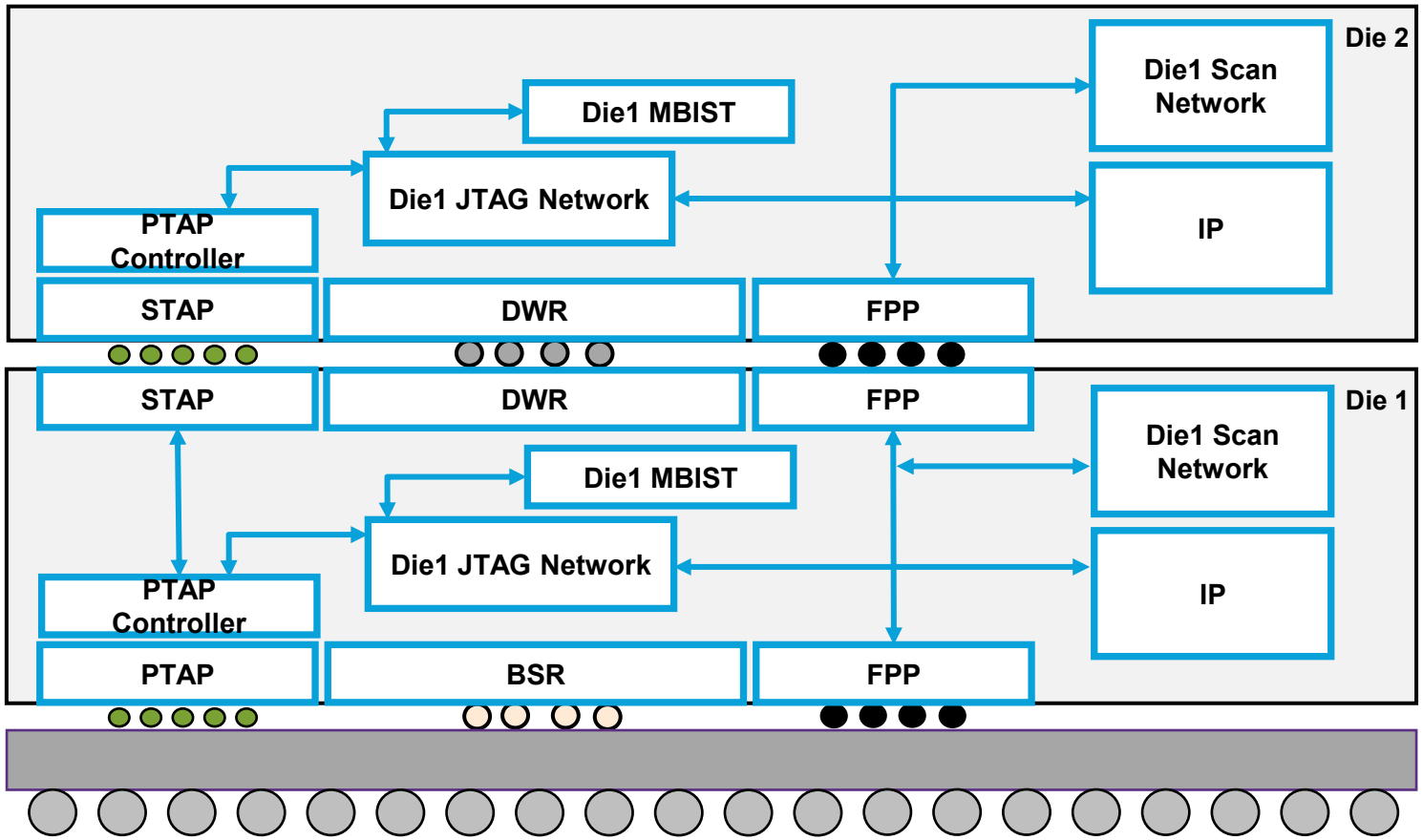


Thermal Evaluation Environment

3D DFT

Implemented with Synopsys tools

- Compliant with IEEE std 1838
- Most test features have been covered



PTAP: Primary TAP
STAP: Secondary TAP
BSR: Boundary Scan Register
DWR: Die Wrapper Register
FPP: Flexible Parallel Port

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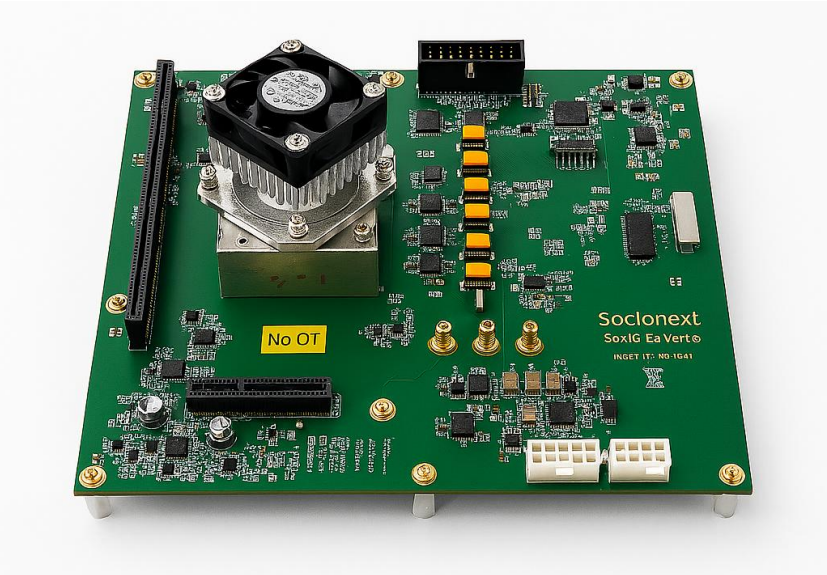
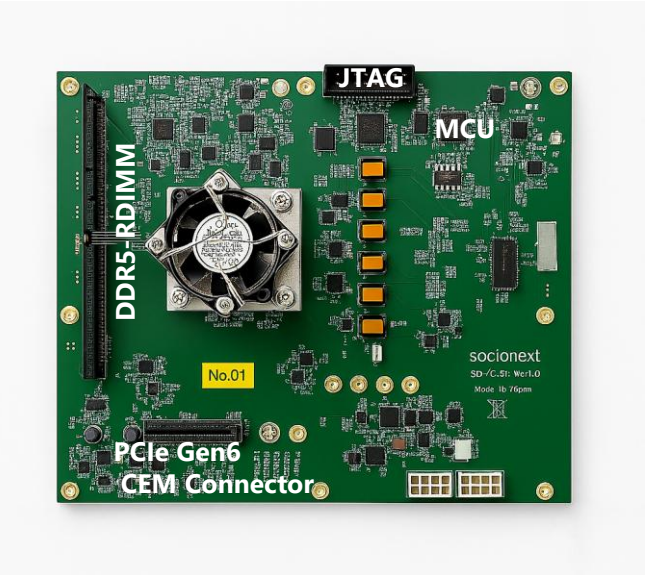
Evaluation

3DIC Test chip and Evaluation Environment

Test chip and Evaluation Board





Test Items and Status

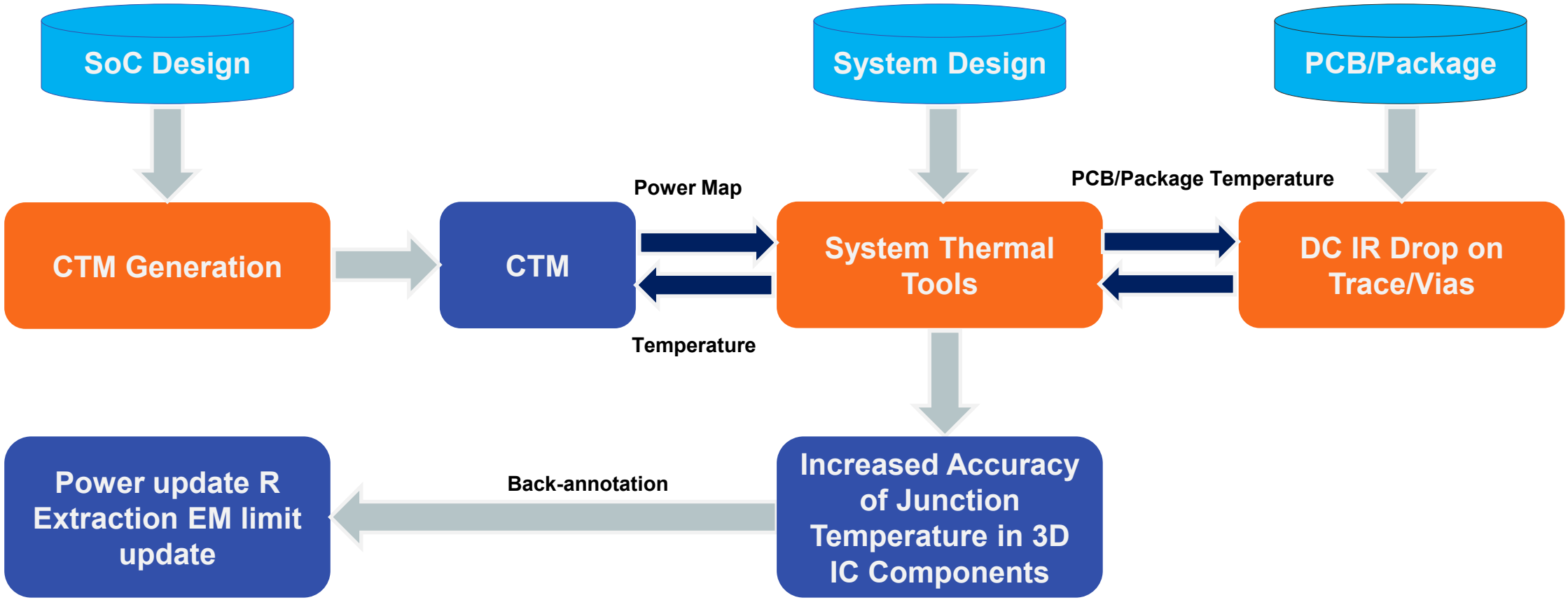
Successful Connection of Top Die and Bottom Die !

- SCP boot-up and AP boot-up ✓**Done**
- DDR function validation and characterization ✓**DDR R/W access Done**
- Linux Boot and run Memtest ✓**Done**
- PCIe Gen6 function validation and characterization ✓**Trying Link-up**
- Thermal evaluation, correlate simulation and evaluation ✓**Thermal sensor access Done**
- Check the DFT circuit compliant with IEEE 1838 on ATE✓**Under preparation**
- Evaluation HSAT on ATE ✓**Under preparation**

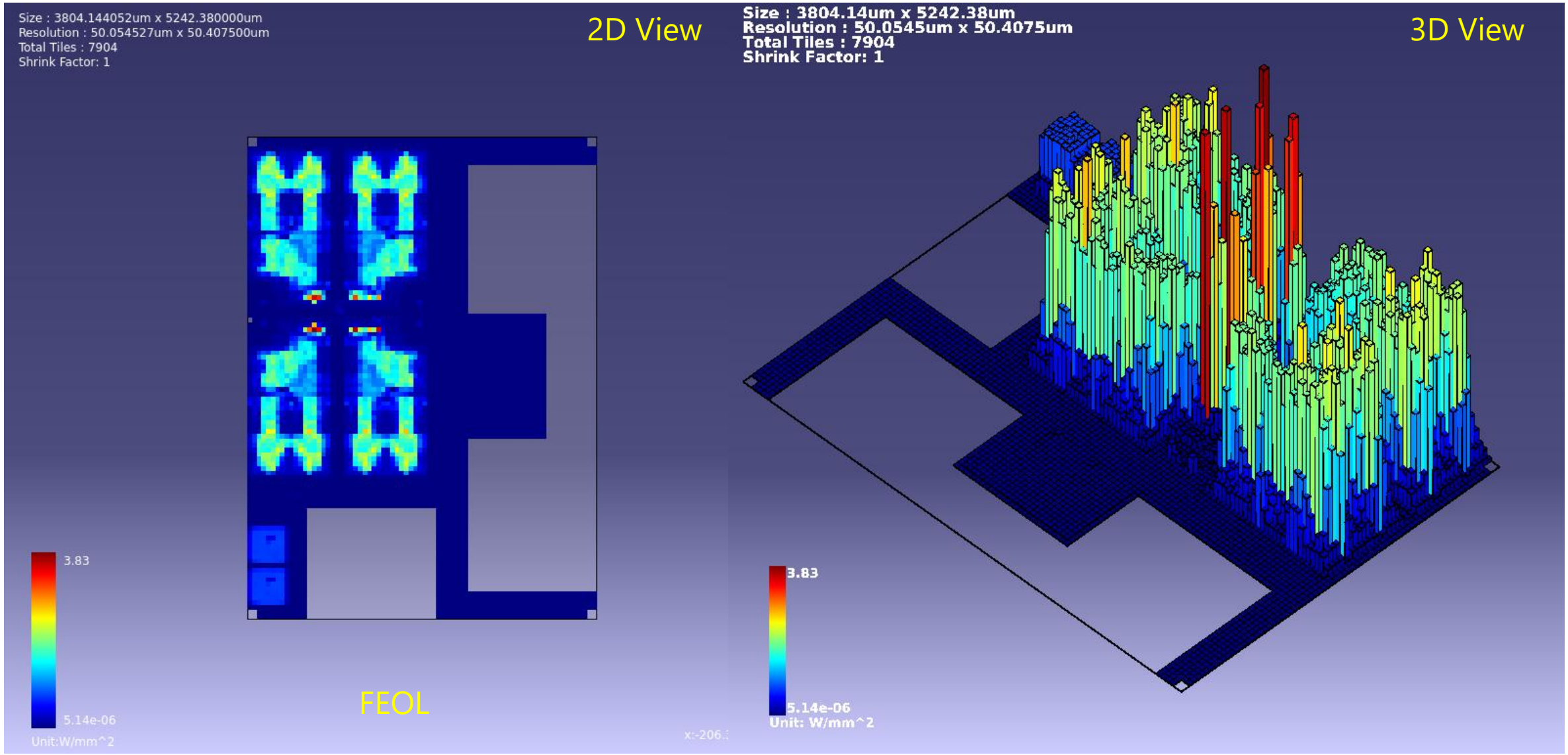
Thermal Analysis with CTM (Chip Thermal Model)

Thermal simulation and validation using test chip

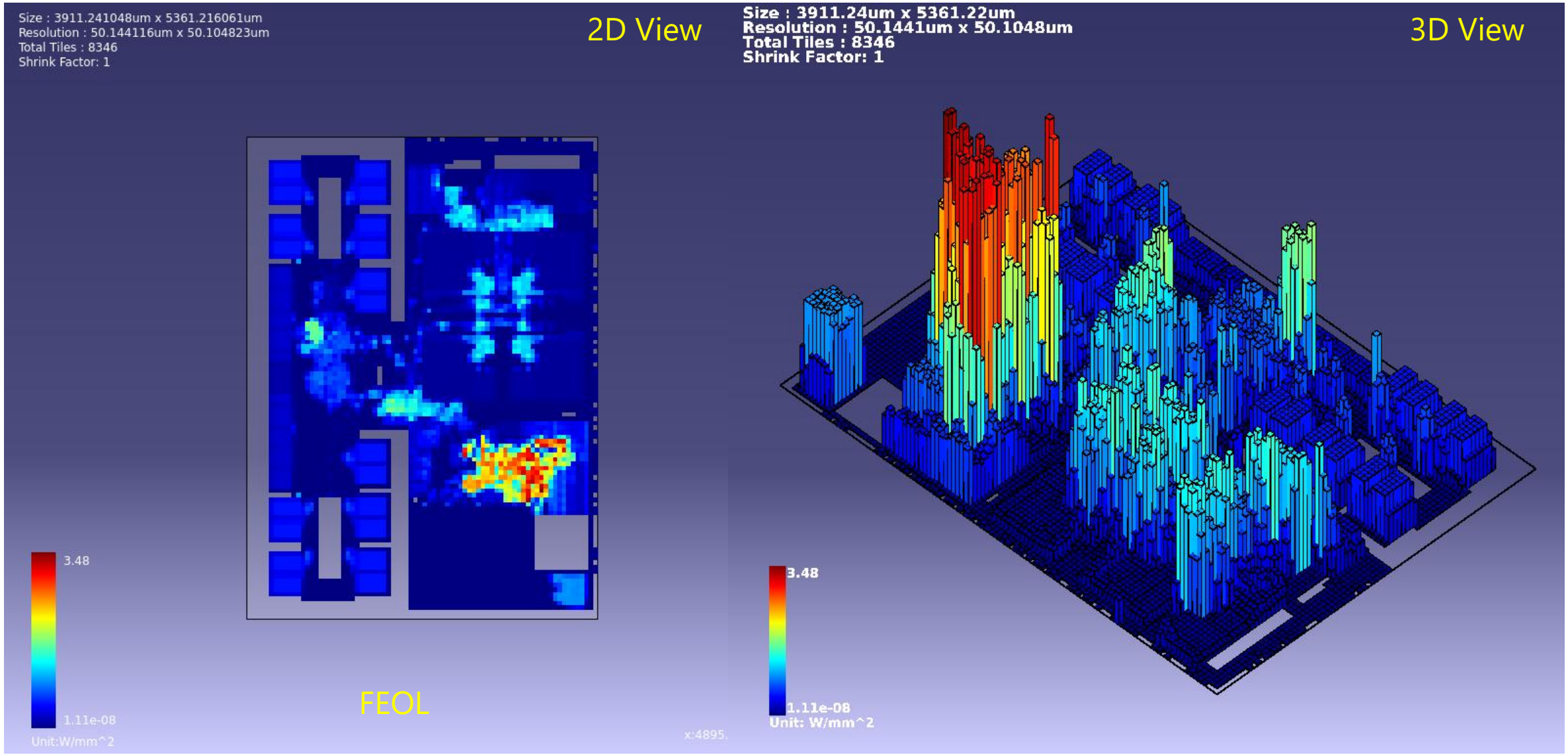
- The CTM technology accurately identifies the hotspot locations and predicts



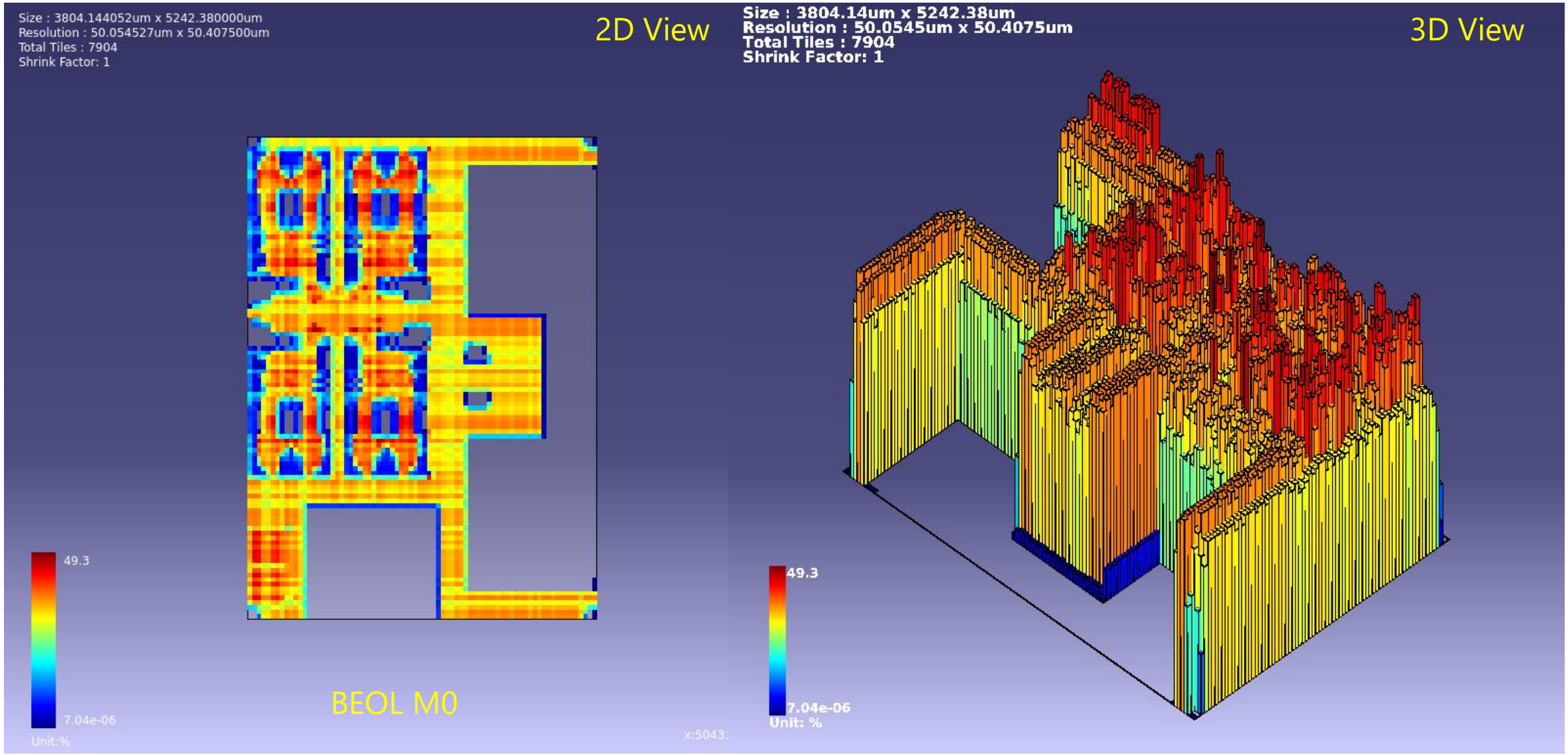
Top Die Power Map



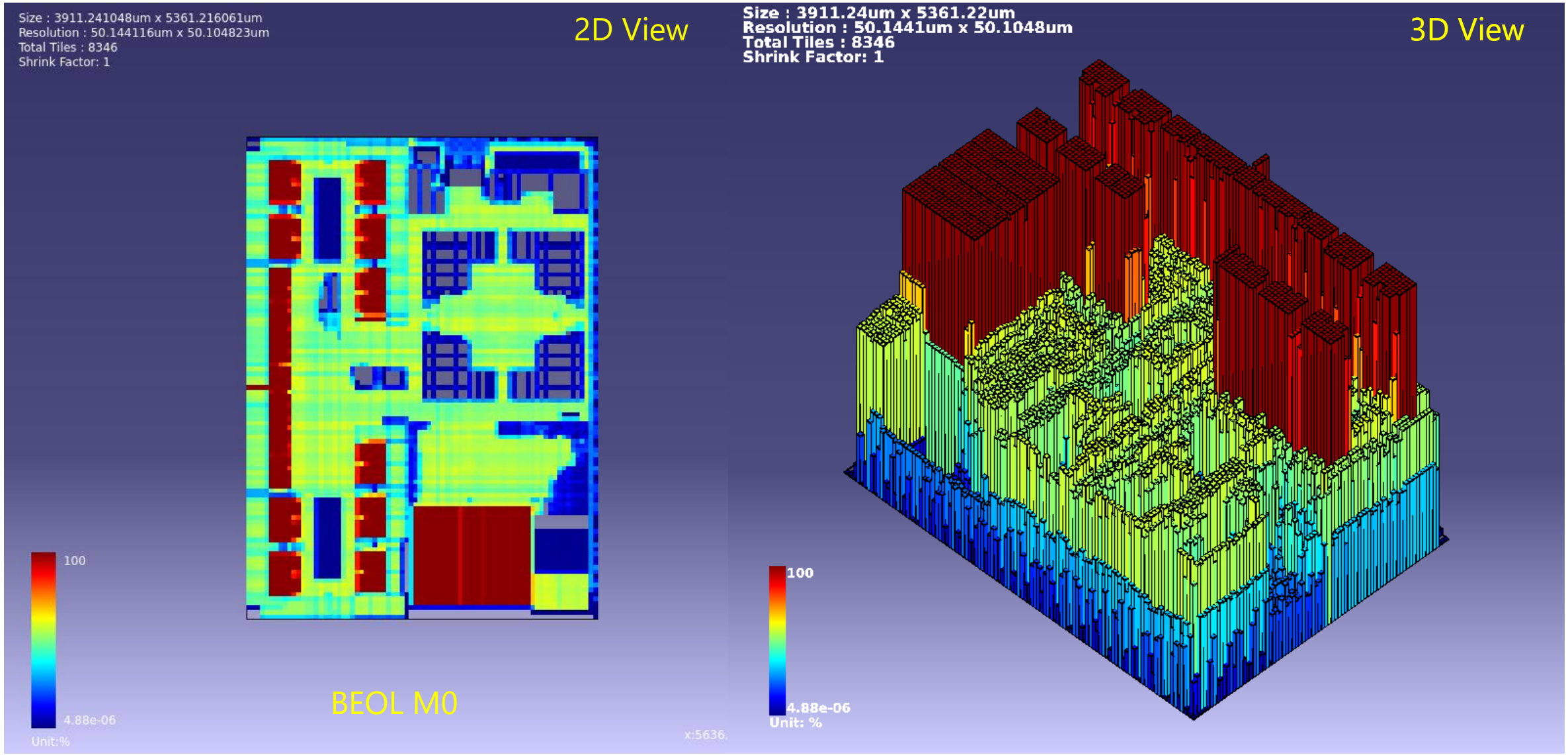
Bottom Die Power Map



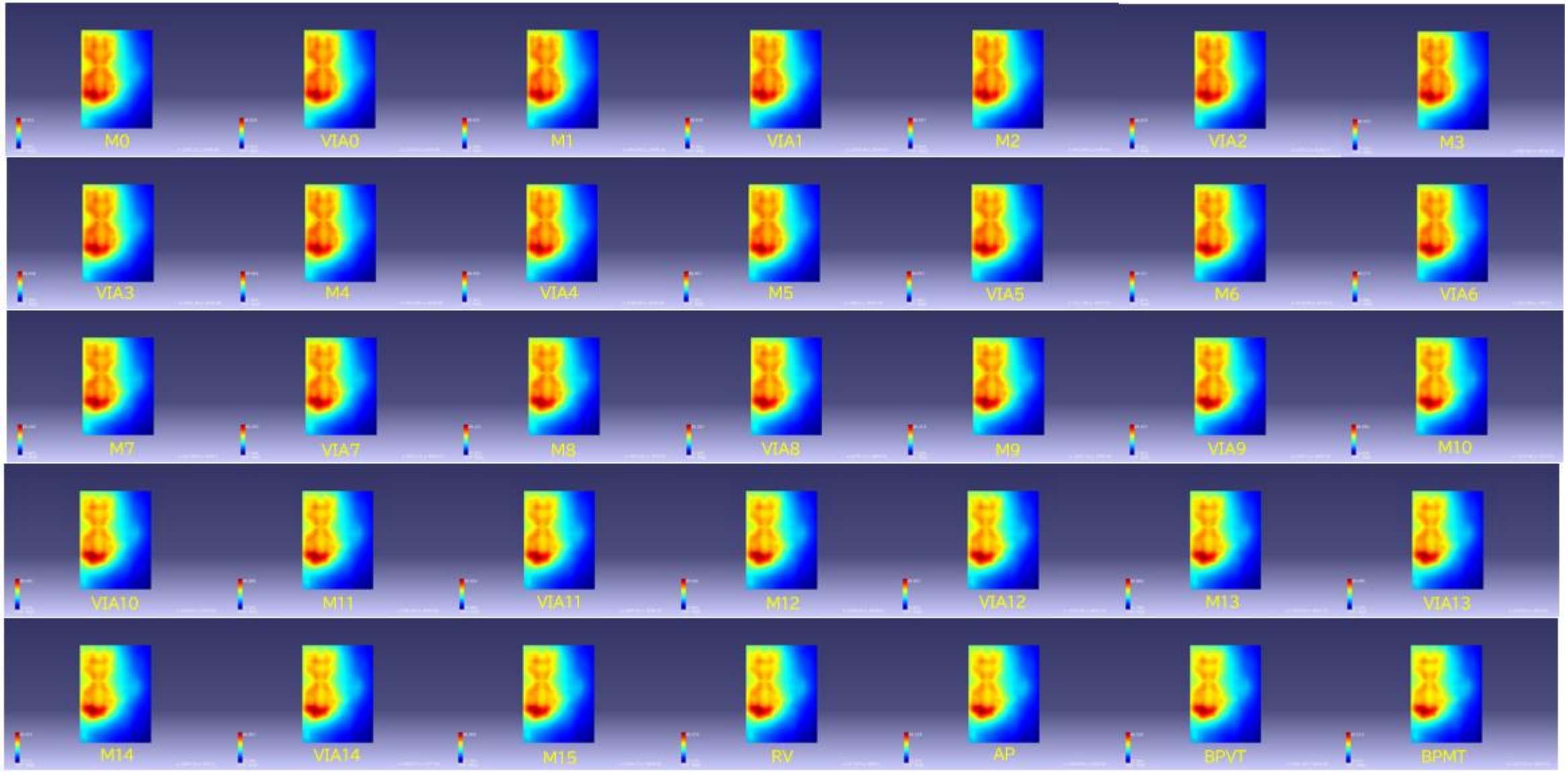
Top Die Metal Density



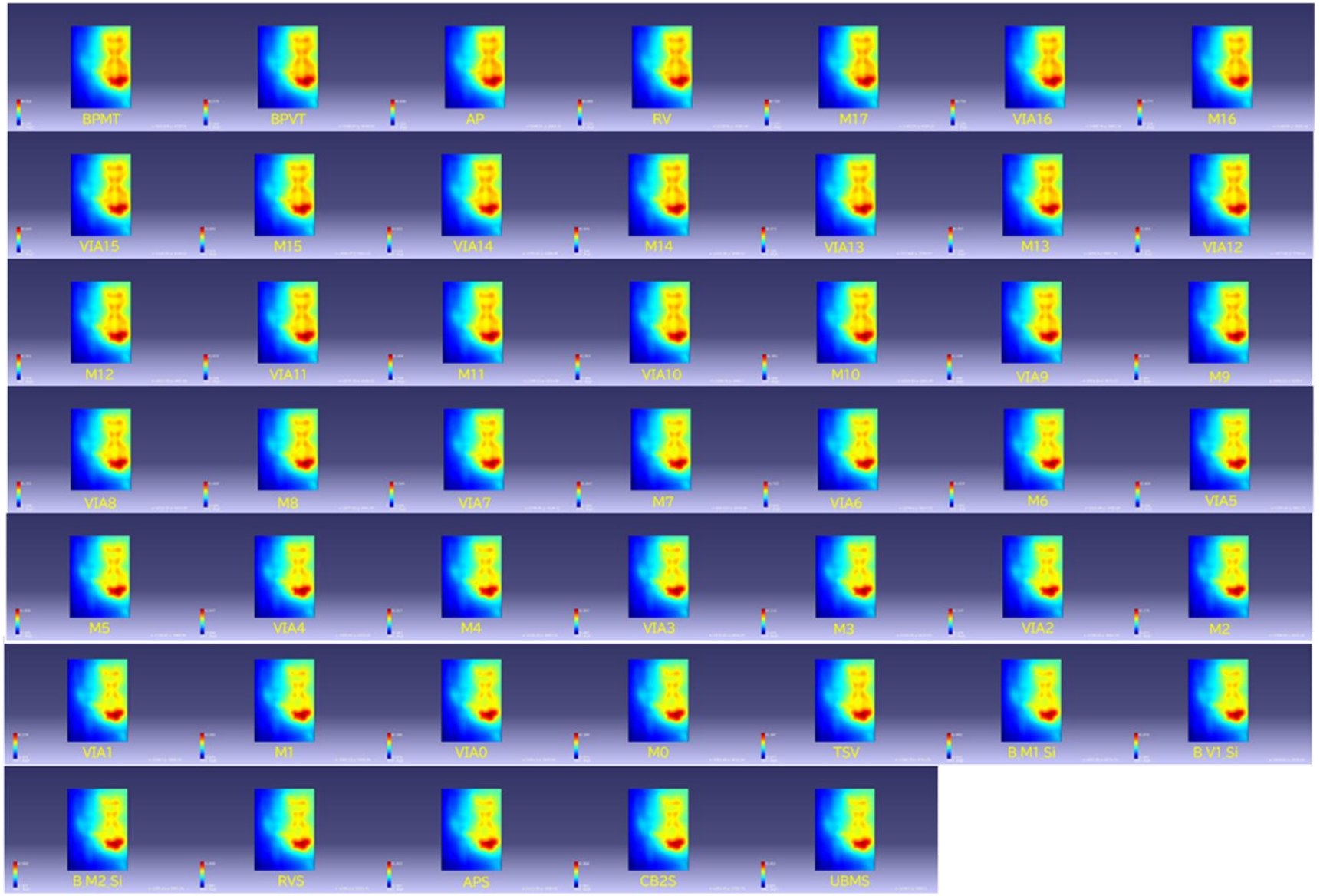
Bottom Die Metal Density



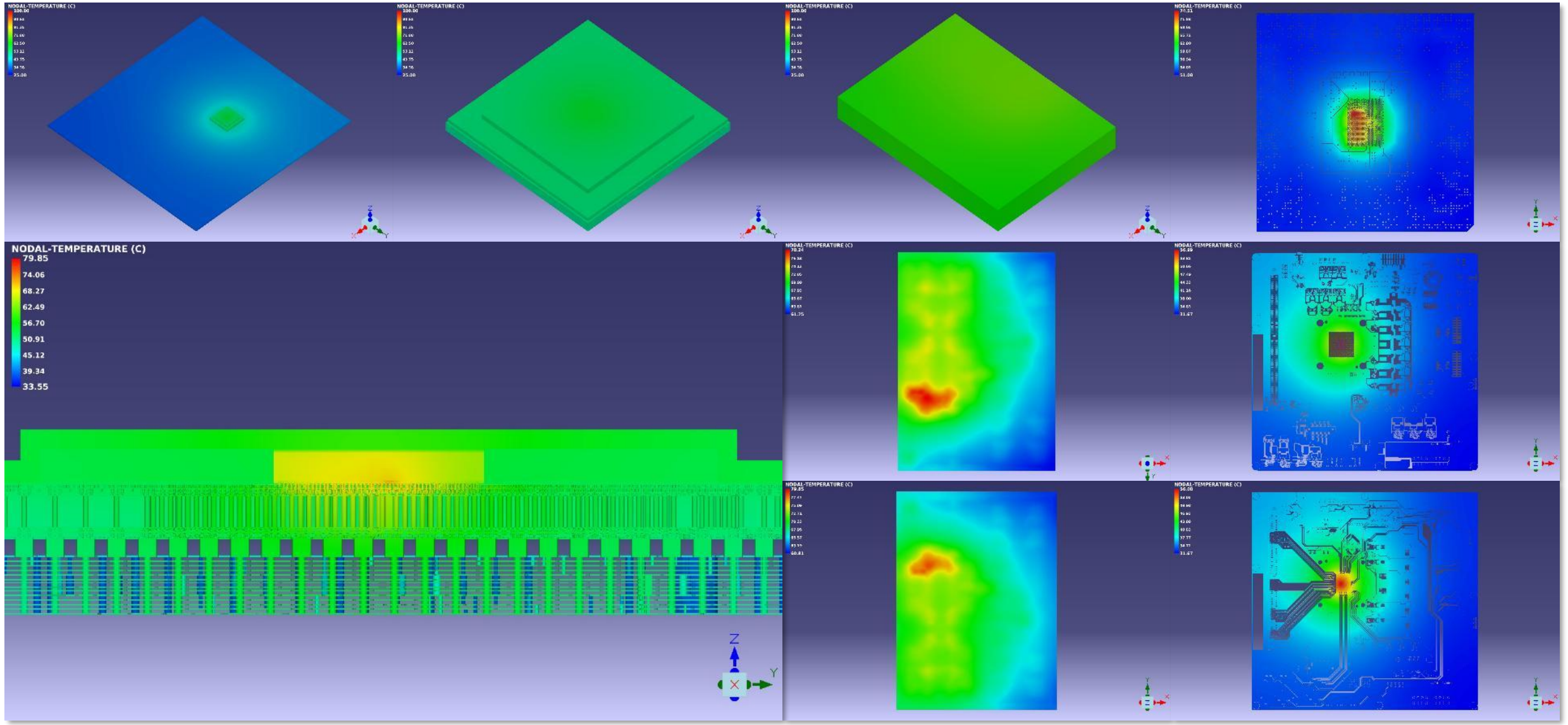
Top Die Chip-Level Thermal Analysis



Bottom Die Chip-Level Thermal Analysis



System Level Thermal Analysis (Chip + Board)



Summary

- **Socionext and Synopsys collaborated to develop a TSMC-SoIC® design solution**
  - Developed logic-on-logic TSMC-SoIC® test chip and tape-out successfully in a very short time
  - Collaborated to build the TSMC-SoIC® design flow
  - Leveraged Synopsys' multi-die solution, including EDA flows and IP
  - Met the requirements for TSMC-SoIC® design with Synopsys' 3D-enabled IP

- **Future Works**
  - Improve the TSMC-SoIC® design flow and methodologies for best TAT & PPA
  - Continue to collaborate and develop new technologies

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The Solution SoC Company

Thank You

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