


**Configuring the Jazz DSP Core
for Application Specific
Requirements**

Oz Levia
CTO

Multi processor SoC Summer School
France 2001

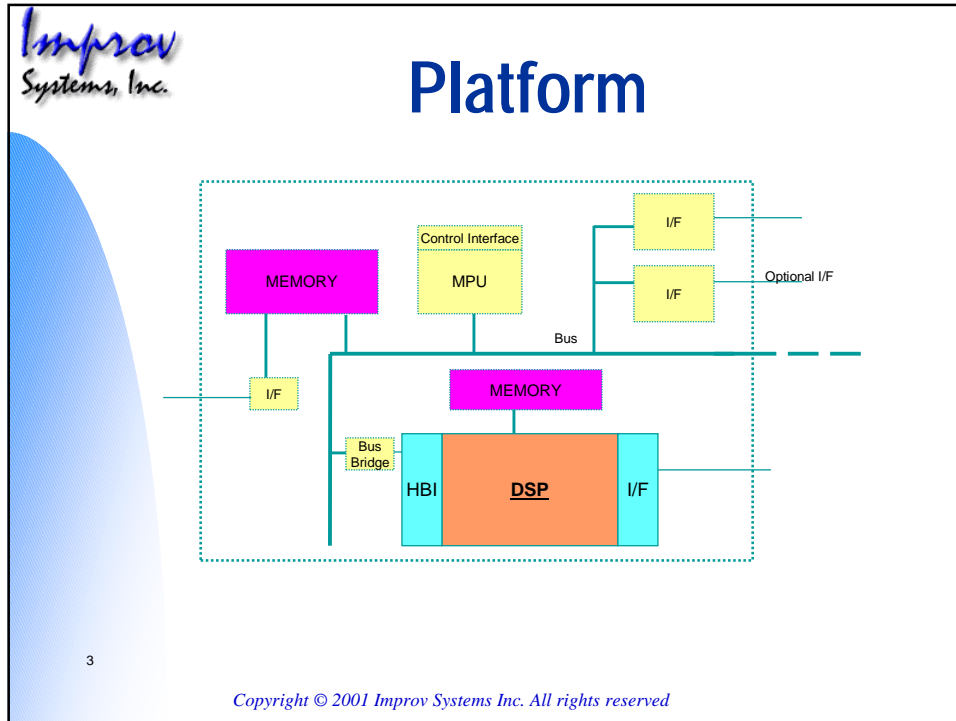


**IC Platform for Data
Oriented Applications**

- Collection of Hardware and Software blocks and IC-IP
- MPU, DSP, Memory, I/O, I/F
- Embedded SW
 - Application 'payload'
 - Control, GUI, I/F
 - RTOS
- Key: Row Capabilities & Integration
 - Cost
 - Power
 - Function
 - Performance

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The diagram, titled "Platform: Requirements", features the same architecture as slide 3. Below the diagram is a list of requirements:

- **MPU: Fixed instruction set**
 - Run protocols, user interface and existing code base
 - Low power
 - Master- Provide RTOS level control and interfaces
- **DSP: Application Specific**
 - Application performance
 - Power
 - Area and cost
- **Memory: Bandwidth, power and area**
- **IO: Standard**


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Focus On The DSP

- In a platform, the DSP is responsible for data processing, the options are:
 - Custom Logic
 - High performance but inflexible
 - Standard programmable parts
 - Known entity
 - Compiler or Assembly code result in OK performance
 - But, one size does not fit all.
 - High cost.
 - Embedded DSP
 - Similar to standard part,
 - “Hard” embedded DSP are Fab captive
 - Multi Processor DSP
 - Little or no compiler support
 - Other Solutions...

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The Goal

Optimize a programmable DSP core(s) in a platform to match the requirements of an **application**

Custom programmable DSP with Compiler and verification tools

Converge Quickly and predictably

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Requirements

- Low power DSP
 - Power consumption is an issue for embedded as well as standard parts
- High performance
 - High volume of data processing
- Programmable
 - Changing application needs
 - Time to market
 - Reuse of IC IP and Application code
- Flexible
 - Fit application size and bandwidth
- Easy to implement
 - Preserve time to market
- Development tools for application deployment
 - Development, verification, debug and optimization

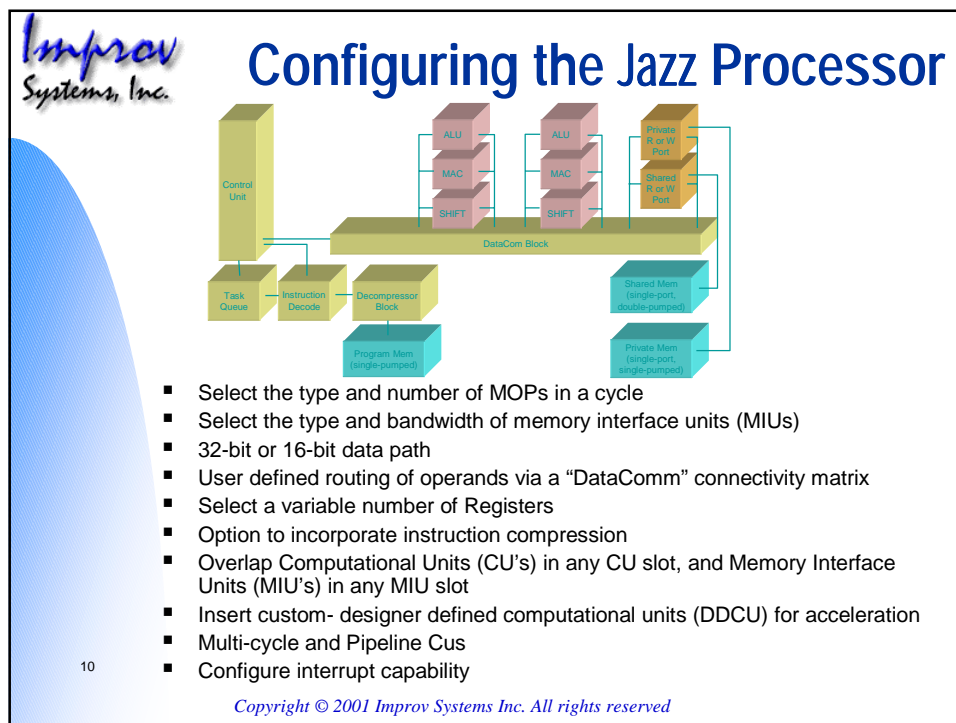
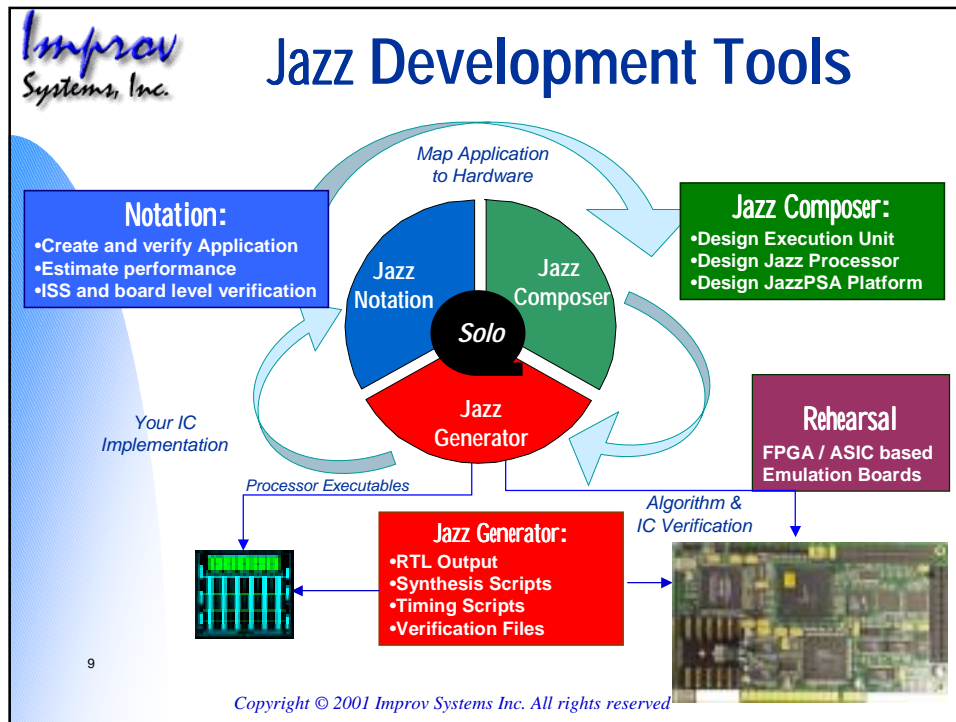
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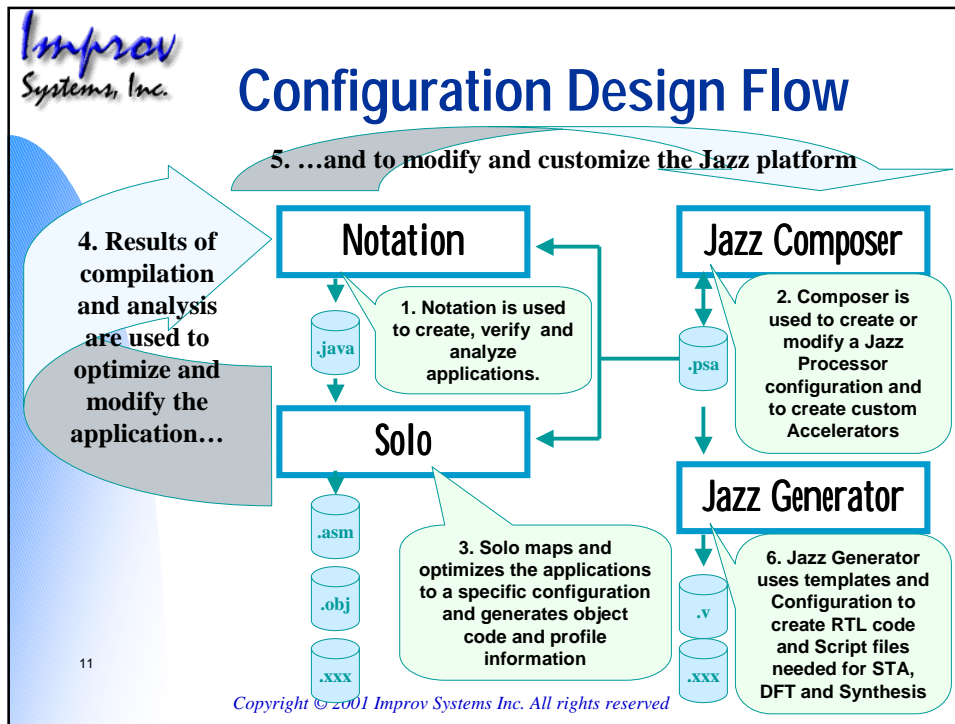
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The Configurable Jazz DSP Processor

- Configurable VLIW DSP
 - Variable number of Micro Operations (MOP) per cycle
 - Variable memory bandwidth
 - Utilizes about 1 sq. mm of die in base configuration,
 - Standard configurations similar to standard DSPs
 - Utilizes less than 0.5 mW/MHz in 0.18 um @1.8v (TSMC)
 - High performance at low clock speed using VLIW approach
 - Requires no custom cells for physical design

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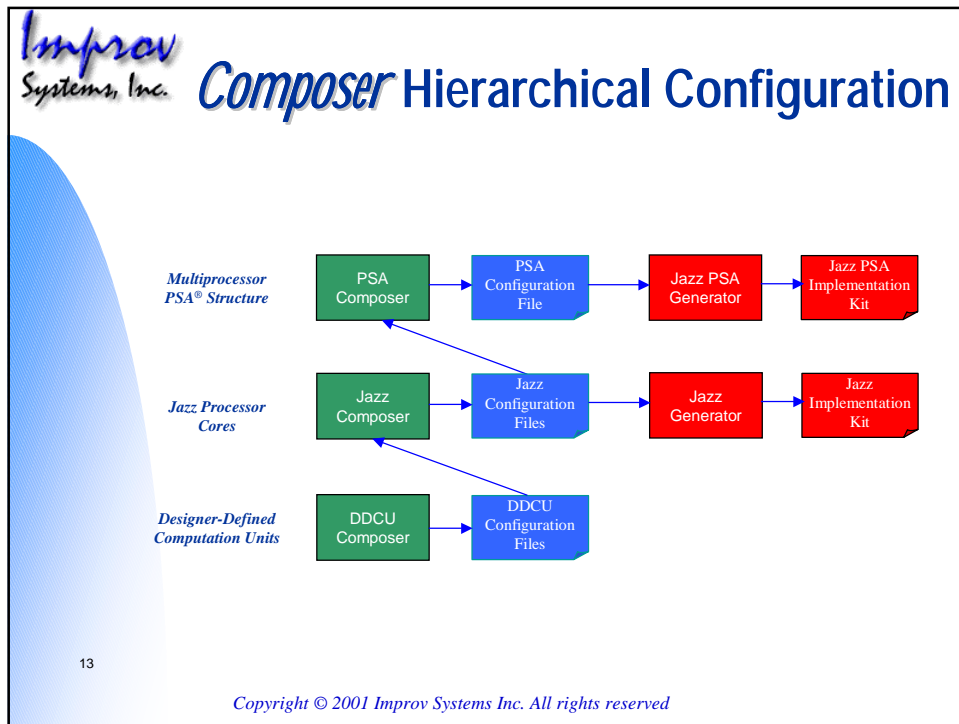
Feedback & Information

- Feedback is used to pinpoint application areas that require optimization...
- And the kind of optimization needed

Screenshot of a code profiler showing a table of code blocks and their execution statistics.

Source	Line	Entered	Exit	Count	Notes
AdaptivePredictor.java	143	1,718,800	4,594,800	execute @ 016F.A3440	18,944
AD726ePredictorGap	058	708,320	3,941,845	execute @ 0726.0738d	18,373
AD726ePredictorGap	587	937,420	3,794,261	execute @ 0726.0738e	33,029
LineToneDetector.java	211	18,800	1,508,800	execute @ 0168.LineTa	4,668
AD726ePredictorGap	188	98,800	818,800	execute @ 0726.0738e	3,871
AD726ePredictorGap	183	8,800	424,800	execute @ 0726.0738d	1,978
AdaptivePredictor.java	178	8,800	294,800	execute @ 016F.A3440	1,817

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Improv Systems, Inc. The Composer Tool

The image shows a screenshot of the "Jazz Composer" GUI. The window title is "Jazz Composer". It features several configuration sections:

- Processor:** Platform: Help, Memory Interface, Descriptors.
- Processor Base Properties:** Processor Name (Jazz_01), Processor Data Width (32), Address Constant Registers, Number of CU Elements, Data Constant Registers, Number of MU Units, Internal Task Queue Active, Priority Task Queue Active, Host Connection, Maximal Task Queue Depth, No. of Constant Registers.
- Computation Unit Properties:** A table listing units with columns for Name, Type, Width, Registers, and Size.

Name	Type	Width	Registers	Size
int	ALU/COND12	32	8	1
int0	SHR/TER12	32	4	2
int1	ALU32	32	4	2
int2	SHR/TER12	32	4	2
int3	MU/32	32	4	2

Buttons for "Add" and "Delete" are visible at the bottom of the table.

- GUI based tool for creating or modifying a DSP Jazz Processor

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Improv Systems, Inc. **Typical Acceleration Blocks**

- Designer Defined Computational Unit (DDCU)
 - Bit Stream oriented
 - Bit level operations
 - “Funny” Arithmetic
 - Multi-stage operations
 - IDCT
 - Filter
 - SIMD

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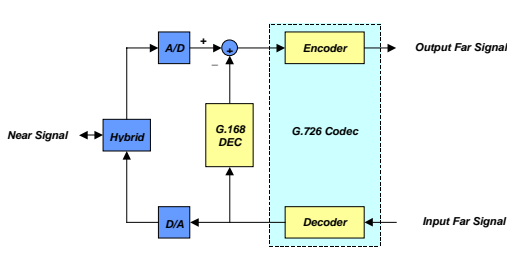
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Improv Systems, Inc. **Example**

- Starting point
 - Application: VoP- G.726 with G.168.
 - Target: Single Jazz DSP.
- Compilation & feedback
 - Baseline results
- Modify baseline *generic* resources
 - What to modify?
- Compilation & feedback
 - What was the effect of the change
- Design and add *custom* resources
 - Where to invest in optimization? Which optimization?
- Compilation & feedback
- ...

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The diagram illustrates the architecture of a Voice over Packet Codec. It shows a feedback loop where a 'Near Signal' is processed by a 'Hybrid' block. The output of the hybrid is split: one path goes through an 'A/D' converter and a summing junction (+) to an 'Encoder' block. The other path goes through a 'D/A' converter and a summing junction (-) to a 'Decoder' block. The 'Encoder' and 'Decoder' are part of a 'G.726 Codec' block. The 'Decoder' also receives an 'Input Far Signal'. The output of the 'Encoder' is the 'Output Far Signal'. A 'G.168 DEC' block is also shown, which receives input from the 'Hybrid' and outputs to the 'Encoder'.

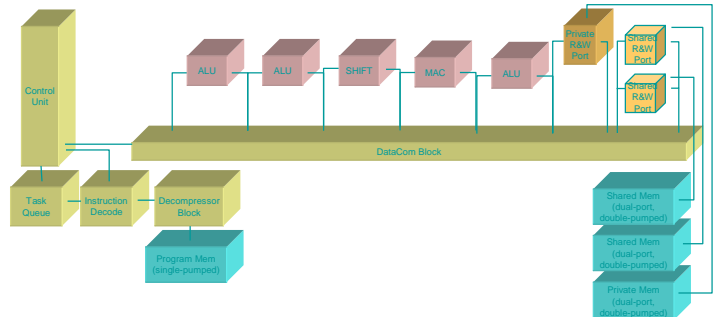
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Voice over Packet Codec

- G.726 Vocoder and G.168 echo cancellation
- This is a portion of a larger application
 - Targeted for the Jazz DSP

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The diagram shows the internal architecture of the Target Jazz DSP. A central 'DataCom Block' (Data Communications Block) is connected to various functional units. On the left, there is a 'Control Unit' connected to a 'Task Queue', 'Instruction Decode', and 'Decompressor Block'. The 'Decompressor Block' is connected to 'Program Mem (single-ported)'. The 'DataCom Block' is connected to three 'ALU' units, one 'SHIFT' unit, and one 'MAC' unit. On the right, there are two 'Private R&W Port' units and two 'Shared R&W Port' units. Below the 'DataCom Block', there are three memory blocks: 'Shared Mem (four-port, 80Kb, 16-ported)', 'Shared Mem (four-port, 80Kb, 16-ported)', and 'Private Mem (four-port, 80Kb, 16-ported)'. The 'DataCom Block' also has a 'Private R&W Port' and a 'Shared R&W Port' connected to it.

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Target Jazz DSP

- VLIW Jazz DSP
 - Three ALU, one MAC, shift unit, four address units
 - All available at each cycle

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Analysis- Where?

- Need a clear picture of what can increase performance
- Look at tasks that are high percent users of cycles

Task	Line	Retired	Cyc	Class	%Total
0726@Predict	691	931,429	4,857,148	improv.o726.o	16.822
0726@Predict	699	780,329	4,248,874	improv.o726.o	15.168
AdaptivePredict	248	1,076,080	4,994,808	improv.o198.ad	14.608
0726@Predict	790	843,429	2,526,267	improv.o726.o	8.821
0726@Predict	650	780,329	1,384,807	improv.o726.o	4.847

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Analysis – What?

- Use information from the compiler: Which resources are constraining the application performance
- First look points to a MAC unit

Task	Line	Retired	Cyc	Class	%Total
0726@Predict	691	931,429	4,857,148	improv.o726.o	16.822
0726@Predict	699	780,329	4,248,874	improv.o726.o	15.168
AdaptivePredict	248	1,076,080	4,994,808	improv.o198.ad	14.608
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0726@Predict	650	780,329	1,384,807	improv.o726.o	4.847

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New Jazz DSP

- One more MAC

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Compile and measure

- Compile application to new target
- Observe results- we gained 10%
- Before:

Engine	Total Cycles	Active Cycles	Idle Cycles	UB
Unallocated	20010010	0	20010010	0%
Engine1	20010010	20010010	0	100%

- After:

Engine	Total Cycles	Active Cycles	Idle Cycles	UB
Unallocated	25281337	0	25281337	0%
Engine1	25281337	25281337	0	100%

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Did MAC unit really help

- Yes

Source	Line	Entered	Cyl.	Class	Weight
0720ePredictorG	687	829,429	4,857,185	improv.g.0720e..	10.421
0720ePredictorG	689	708,329	2,881,845	improv.g.0720e..	15.591
0720ePredictorG	709	843,429	2,530,387	improv.g.0720e..	10.889
0720ePredictorG	698	708,329	2,124,887	improv.g.0720e..	0.485
AdaptivePredictor	248	1,018,808	2,832,800	improv.g.0180Ad.	0.020
LineToColDetector	211	18,808	1,024,800	improv.g.0180L1.	4.850

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Analysis- Where else can we improve?

- Function LMB+1 is called in many places
- Bit level operation is 'emulated' by ALU
- Can be performed by HW unit

Source	Line	Entered	Cyl.	Class	Weight
0720ePredictorG	687	829,429	4,857,185	improv.g.0720e..	10.421
0720ePredictorG	689	708,329	2,881,845	improv.g.0720e..	15.591
0720ePredictorG	709	843,429	2,530,387	improv.g.0720e..	10.889
0720ePredictorG	698	708,329	2,124,887	improv.g.0720e..	0.485
AdaptivePredictor	248	1,018,808	2,832,800	improv.g.0180Ad.	0.020
LineToColDetector	211	18,808	1,024,800	improv.g.0180L1.	4.850

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Create a DDCU

- DDCU: Designer Defined Computational Unit
- Function: ALU with special operations for LMB+1.
- Specifications
 - A class definition of the operation(s).
 - Each method defines an Op-code
 - DDCU can include multiple Op-codes
- Integration to application
 - Method call(s)
- Integration to Jazz
 - Configuration with composer
 - Add a CU

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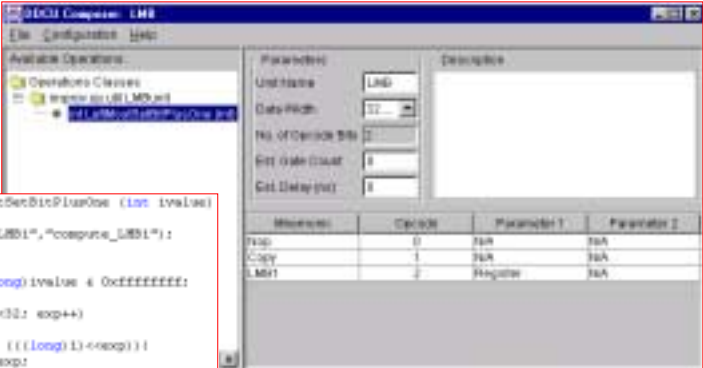
Creating a DDCU

- Use Composer to create DDCU

```

public int LeftBorderBitPlusOne (int value)
{
    UndefinedOp("LMB1", "compute_LMB1");
    PSA.Inline();
    int exp;
    long value = (long)value & 0xffffffff;

    for (exp=0; exp<32; exp++)
    {
        if (value < (((long)1)<<exp))
            return exp;
    }
    return exp;
}
                
```



Operation	Op-Code	Parameter 1	Parameter 2
Plus	0	RA	RA
Copy	1	RA	RA
LMB1	2	None	RA

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Add DDCU to Jazz DSP

- Add the new LMB unit into a Jazz DSP Processor
- New Jazz Processor now has Custom unit.

Computation Unit Properties

Name	Type	Width	Regist
al1	ALU32	32	4
al2	ALU32	32	4
al0	ALUCOND32	32	4
mp0	MAC32	32	4
sh0	SHIFT32	32	4
mp1	MAC32	32	4
LMB0	LMB	32	4

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New Jazz DSP

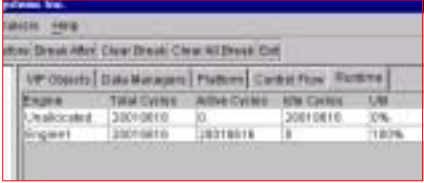
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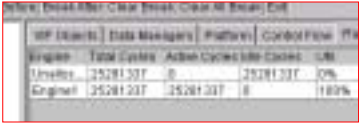
Compile and measure

- Compile application to new target
- Observe results
- Before



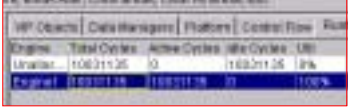
Engine	Total Cycles	Active Cycles	Idle Cycles	LR
Unallocated	20010610	0	20010610	0%
Engine1	20010610	18318618	8	180%

- With MAC



Engine	Total Cycles	Active Cycles	Idle Cycles	LR
Unallocated	25281337	0	25281337	0%
Engine1	25281337	25281337	0	100%

- With LMB & MAC



Engine	Total Cycles	Active Cycles	Idle Cycles	LR
Unallocated	10821126	0	10821126	0%
Engine1	10821126	10821126	0	100%

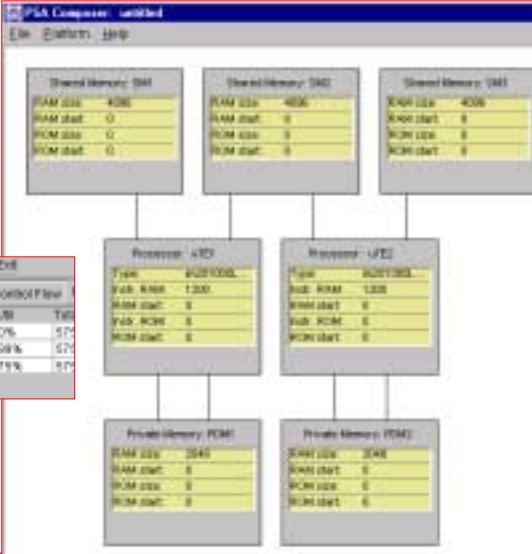
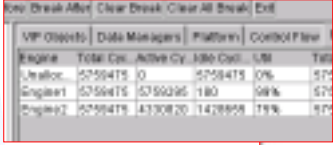
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What next?


- One Processor is doing 'all it can'
- Lets try two processors
 - One processor with LMB
 - One processor without
- Results:

Engine	Total Cycles	Active Cycles	Idle Cycles	LR
Unalloc	5759475	0	5759475	0%
Engine1	5759475	5759295	180	98%
Engine2	5759475	1430820	1428658	19%

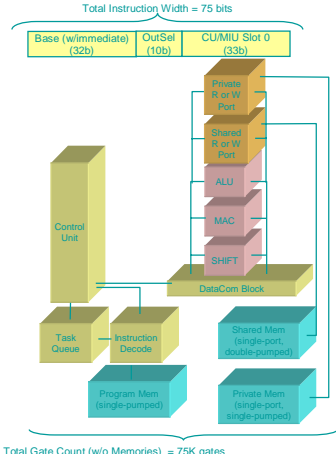
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Jazz 2010 – Single MAC Processor


- Low End, Single instruction slot / multi-Computation Unit Configuration
- RISC-Like Processor with DSP Extensions
- Equivalent to DSPG Teak-lite, TI C54x, StarCore SC110, Intel/ADI XScale



Total Gate Count (w/o Memories) = 75K gates

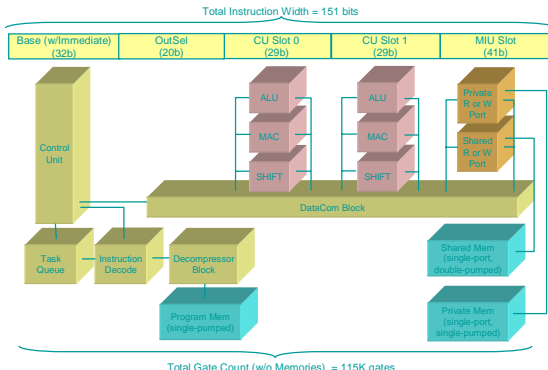
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Jazz 2020 – DUAL MAC Processor

- Medium Range DSP for most new DSP applications in the market including VoP, Encryption, Edge Networking, 3G Wireless
- Comparable to TI C55x, StarCore SC120, 3DSP, DSPG Teak



Total Gate Count (w/o Memories) = 115K gates
(TSMC 0.15 um)

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Jazz 2040 – Quad Mac Processor

Total Instruction Width = 251 bits

Total Gate Count (w/o Memories) = 170K gates
(TSMC 0.15 um)

- High end processor for performance intensive applications
- Competes with TI C62x, C64x, StarCore SC140, etc.

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Acappella - PacketCable Reference Platform

- VPS could be a stand alone chip or used as a core integrated into an SoC

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Conclusions

- VLIW DSP processor architecture with High performance
- Flexible architecture to meet the needs of applications
- Configuration file guide the tools chain in mapping to specific target
- Fast, tight loop: Compile, measure, change, Compile...
- Small changes in DSP can lead to great differences in performance
- It is critical to have the right feedback
 - Feedback is used to guide modifications
- The designer is the most important part of this loop

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