Will 3D stacking of ICs enable to continue Moore's momentum in the 21st century?

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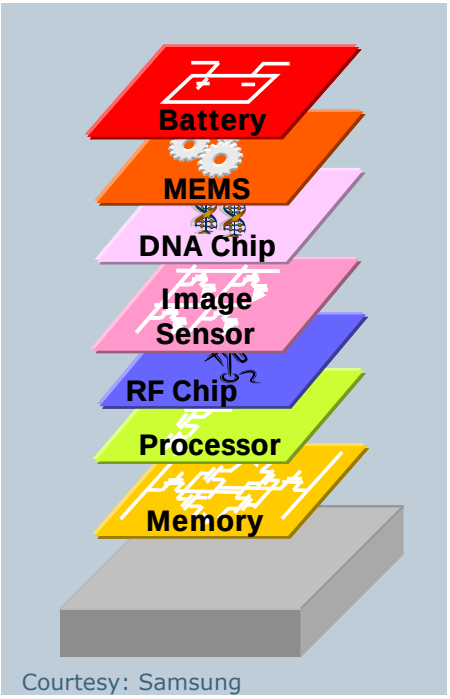
Vice-President Nomadic Embedded Systems
Professor Katholieke Universiteit Leuven

imec

3D Integration – Many System Opportunities



Courtesy: Samsung

Maintaining Moore's momentum
- increase functionality with number of additional layers

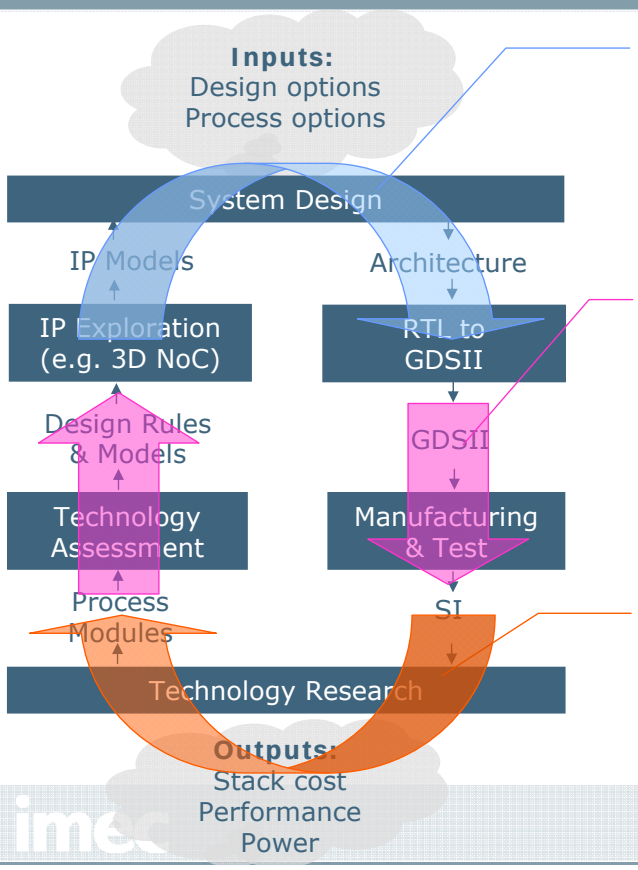
3D resolves the interconnect performance limitations
- the on-chip interconnect length and related repeater cost

Heterogeneous integration
- build an integrated system with dedicated logic, SRAM, DRAM, FLASH, RF technologies
- add new sensors, batteries, etc.

More modular & scalable design
- add new standardized components, replace existing ones with better performing ones

Sleek form factor
- 1mm^3 corresponds to >100Mbit SRAM cells

PathFinding @ The Core of introducing 3D



Architecture Exploration for 3D
- To find the technology/design sweet-spot (including cost modeling)
- To provide IP necessary for 3D design and understand its technology requirements
- To analyse the impact of 3D on architectures

3D Technology Assessment & Prototyping
- To demonstrate process steps and basic integration
- To demonstrate a reliable and yielding base-line process
- To establish a modeling environment, basic design kit and design rule check
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3D Process Technology R&D
- To R&D 3D technologies for reliable stacking and interconnection of heterogeneous components
- To outperform existing 2D technologies in cost, power, performance and time-2-market

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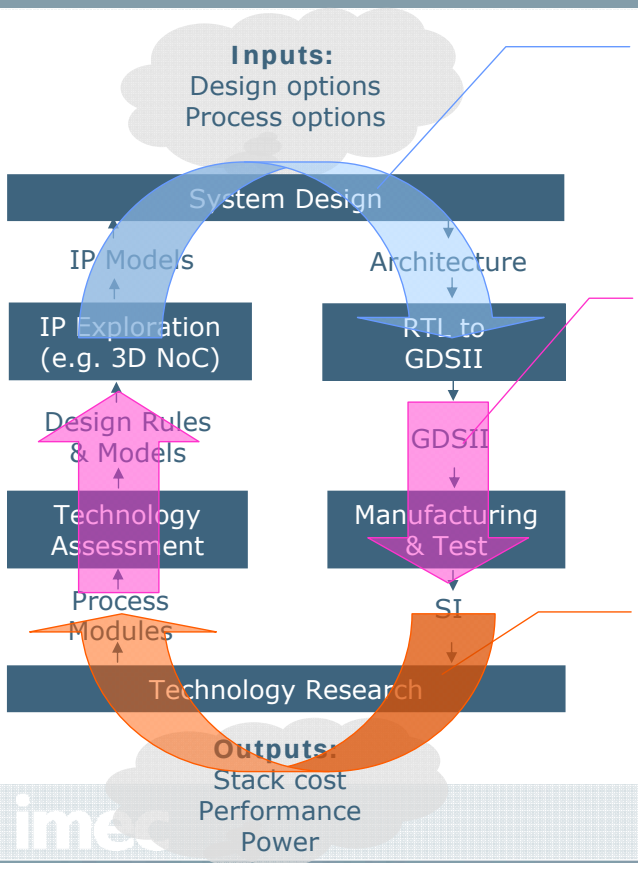

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3D TSV Technology Roadmap

Technology Programme	3D-WLP TSV			3D-SIC Cu-nails TSV			3D-IC Sub-µ TSV	
Via size	50 um	25 um	10 um	5 um	2 um	1 um	500 nm	100 nm
Via pitch	80 um	40 um	20 um	10 um	5 um	4 um	1 um	200 nm
Wafer thickness	100 um	50 um	30 um	20 um	15 um	10 um	Active layer only - SOI	
				50 um	30 um			
Interconnect Hierarchy	Bondpad (0-level)			Global level	Intermediate level		Local interconnect	

- Use of standard Si
- Multi-source possible
- Post-foundry process
- D2D or D2W stacking
- Mainly parallel process
- Strongly Cost driven

IIAP 3D-WLP

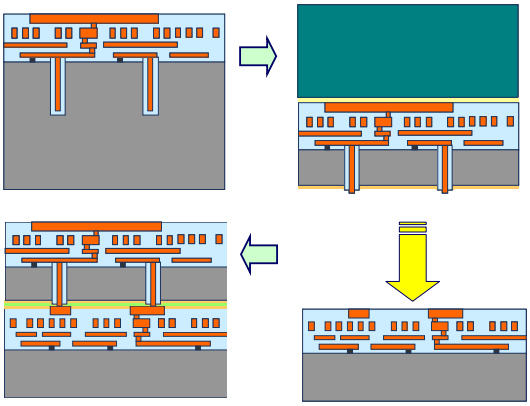
- Cu nail process in foundry
- Thinning/stacking post-foundry process
- D2W or W2W stacking
- Key: D2W/W2W alignment accuracy, speed and yield
- Mainly parallel process

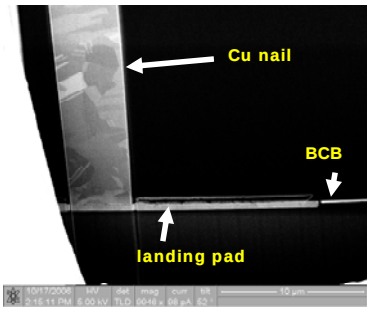
IIAP 3D-SIC

- Fully foundry level process
- Requires use of SOI wafers
- only W2W stacking possible
- Extreme W2W alignment accuracy required
- Sequential process flow
- Compound yield issues

3D Interconnect Technology Developments at IMEC

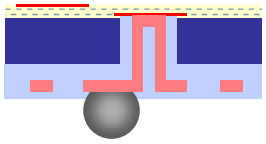
3D-SIC Cu-nail TSV

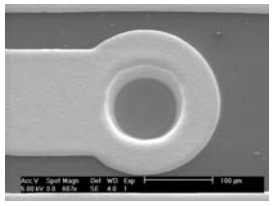


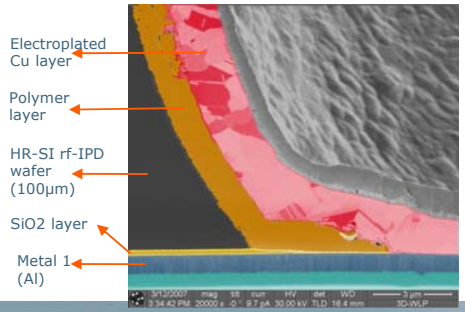


3D-WLP

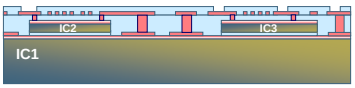
Cu / polymer TSV

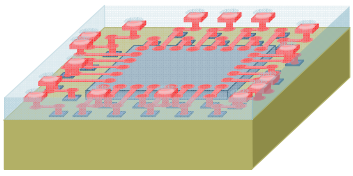


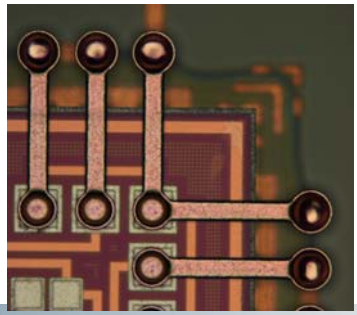




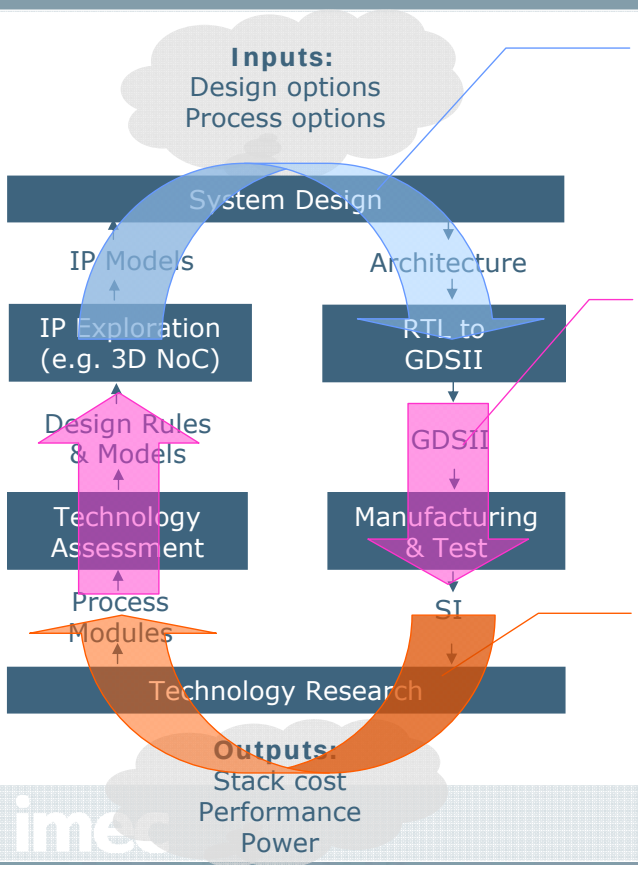
Ultra-thin Chip stacking







PathFinding @ The Core of introducing 3D



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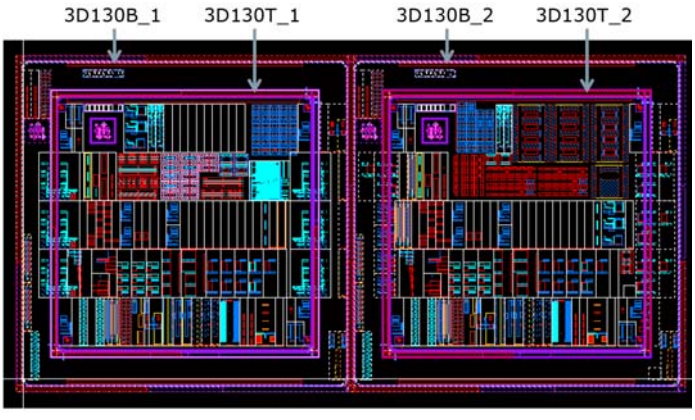
Test Chip Design

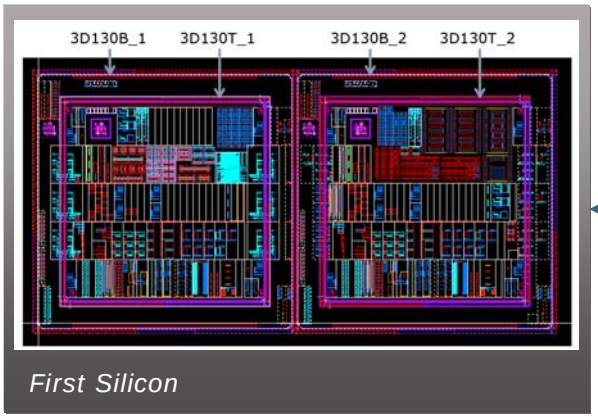
- Test Structures for Design Rule Assessment
  - TSV characteristics: capacitance, resistance, yield, stack alignment, …
  - Impact of TSV and of relative process on transistors
  - Impact of TSV and of relative process on wires
  - Diode-based thermometers, hot-spot heaters to be placed in different chip locations
  - Structures for processing and for std tests
  - RF test structures
  - Dedicated test structures by our partners
  - Small 3D circuits (e.g. ring oscillator with stages distributed in different chip level, …)

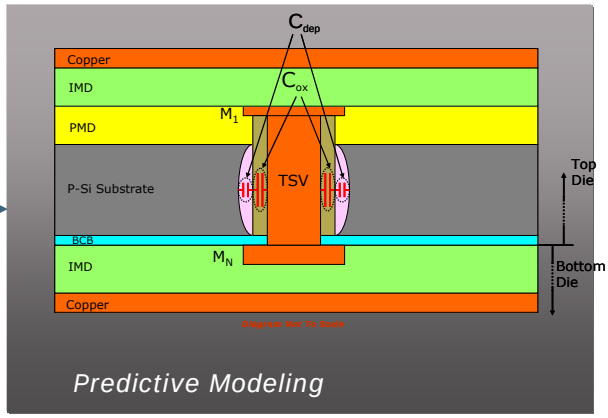


- For 200mm wafers (2 metal layers - 130nm platform technology)
- TSV: Via diameter: 5um/Via pitch: 10um
- D2W and W2W possibilities at the same time

Design rule and model assessment of TSVs

Basic process modules knowhow





Design rules & models

PathFinding flow & Basic Design Kit

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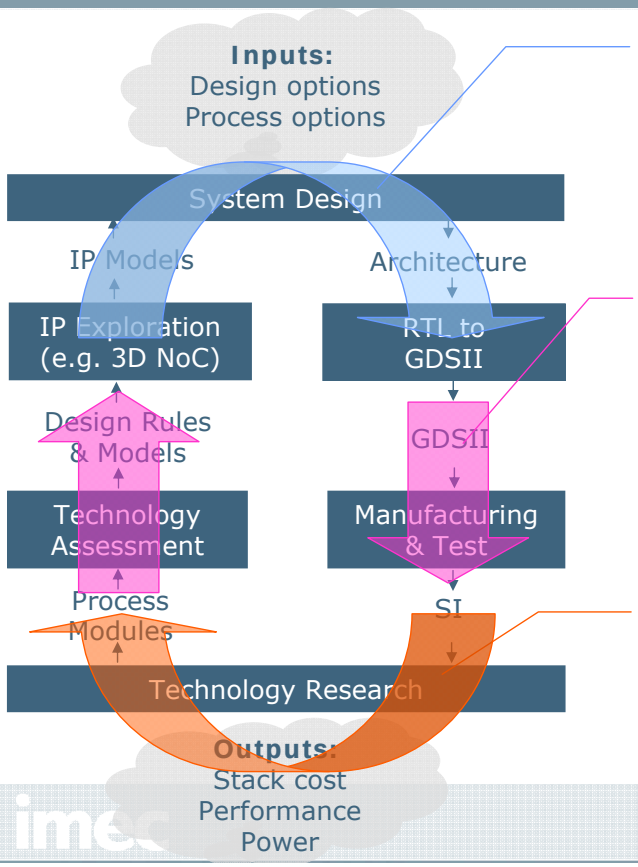

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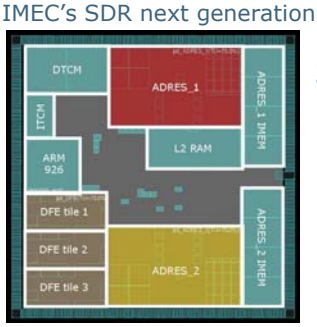
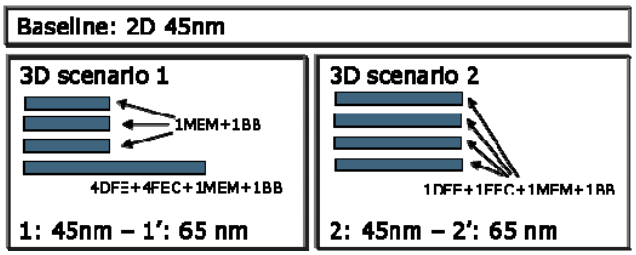
Path finding - a first illustration

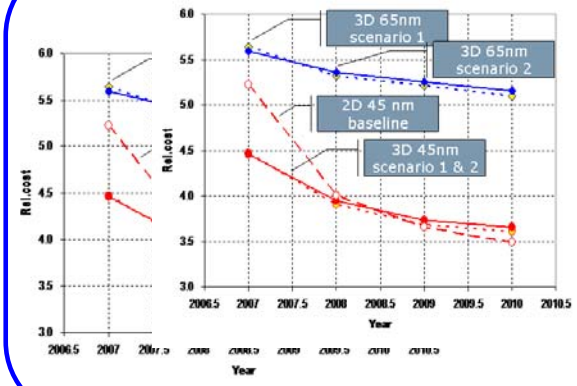
IMEC's SDR next generation



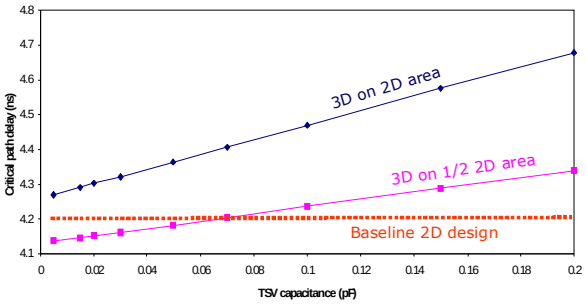
3D Integration Scenarios



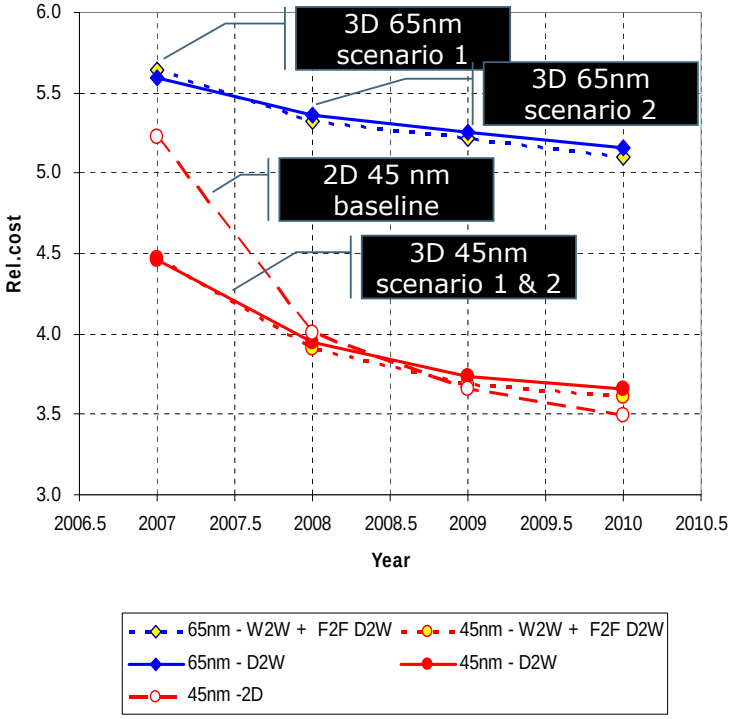
Preliminary cost analysis



Performance Analysis for Various Technology Parameters

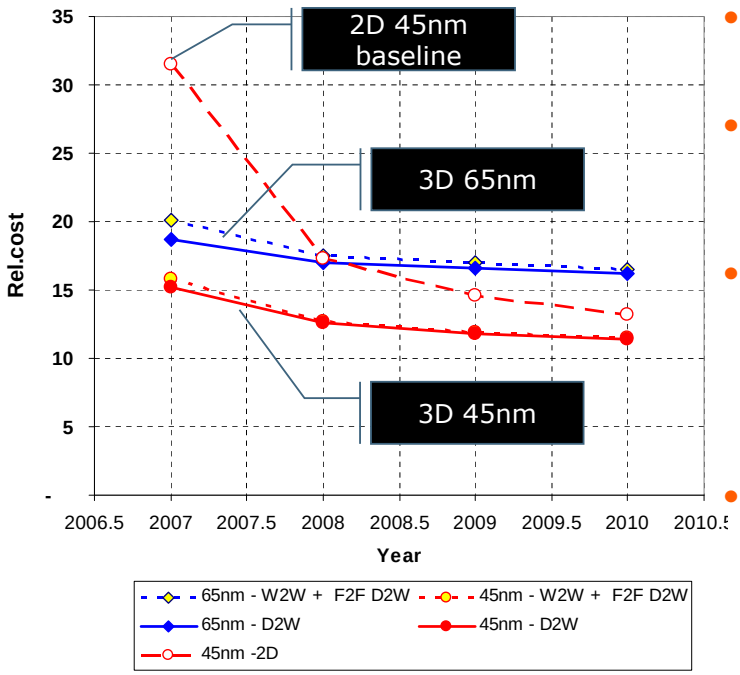


Manufacturing cost of 3D SIC



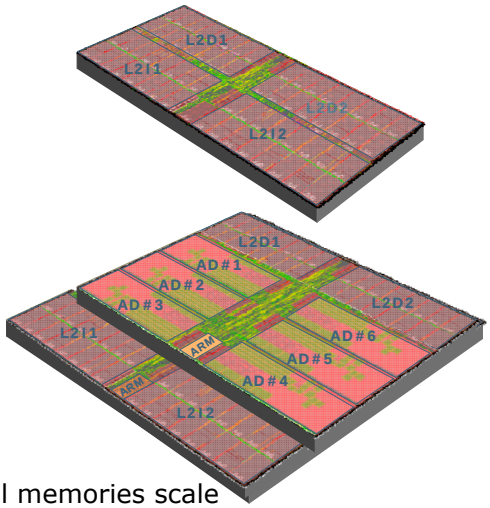
- Assumptions
  - Area of 2D 45nm baseline SDR: 34mm^2
  - 3D technology: TSV 10µm
  - Homogeneous technology layers, custom fabricated
  - Manufacturing cost is dominant
- Conclusions
  - 3D using older (65nm) technology is never attractive compared to 2D 45nm baseline
  - 3D using 45nm technology is only attractive on the short term
- But ...

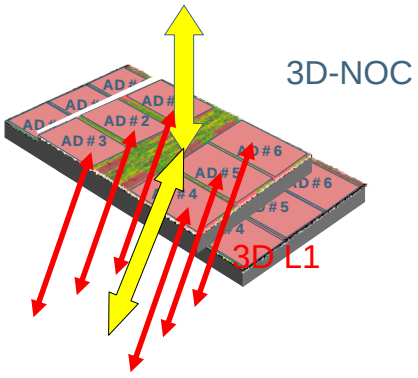
Manufacturing cost of 3D SIC



- Assumptions
  - Area of 2D 45nm baseline SDR: 102mm^2
- Becoming attractive for $
  - Lower yield loss (smaller dies)
  - Importance increases for scaled technologies
- More opportunities need to be explored:
  - Heterogeneous technologies
  - Smaller volumes when NRE is dominant
  - Commodity components
- Top-down path finding allows co-exploration of technology and design
  - In light of cost

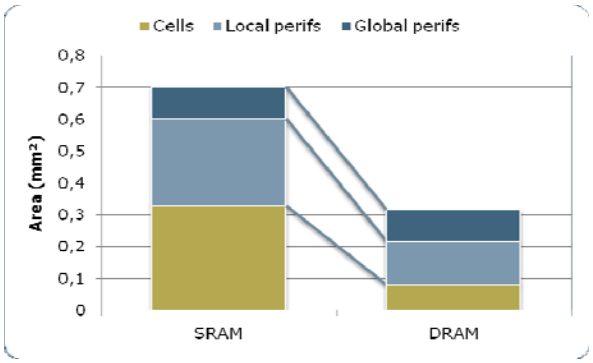
3D DRAM to substitute badly scaling SRAM





- Small memories scale badly below 45nm due to process variations
- Companies ask us: "provide us with possible alternatives"?

3D DRAM as replacement for embedded SRAM - Preliminary results



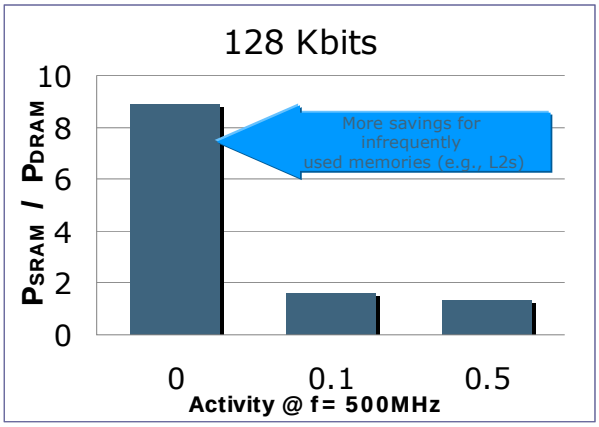
128kB memory@500Mhz

Area:

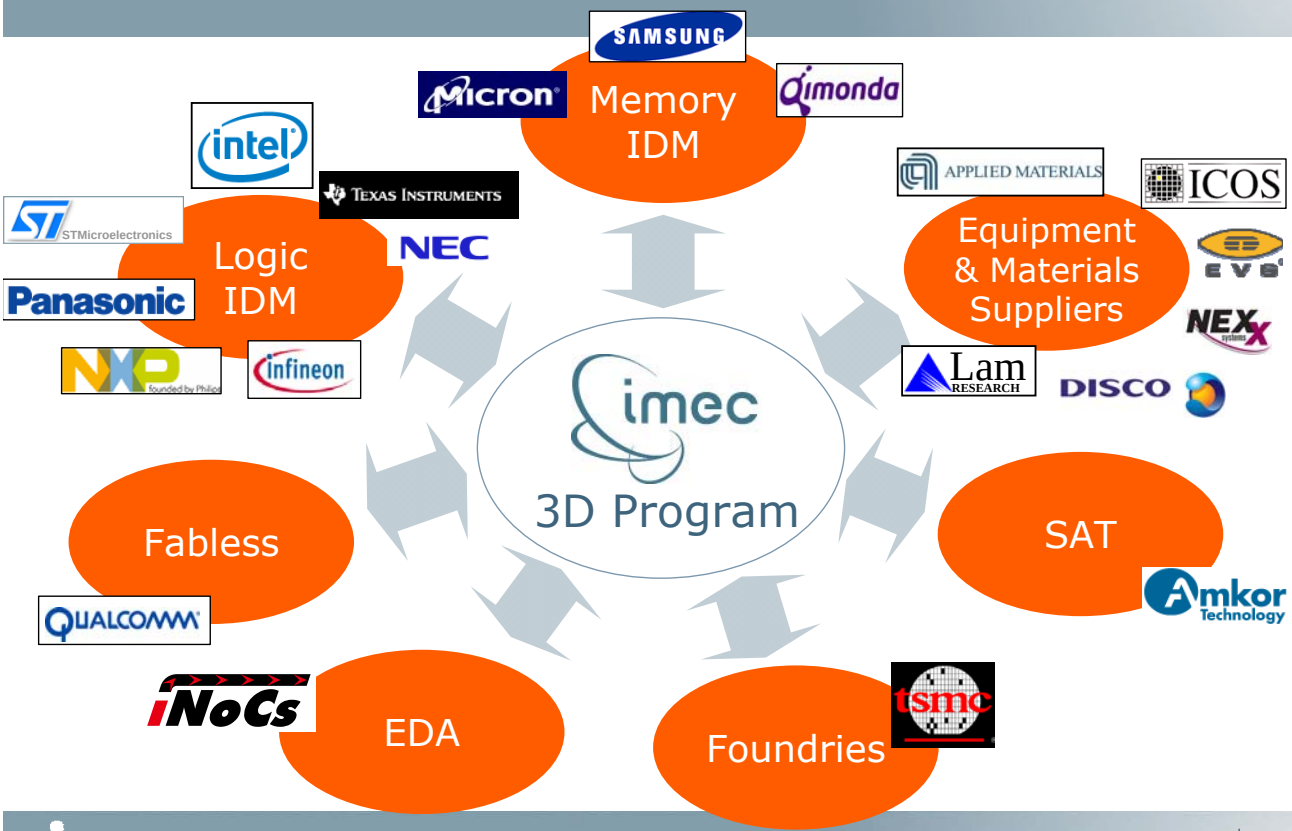
- DRAM cells are 10x smaller compared to SRAM
- More than 2x area reduction by just changing the cell on a SRAM matrix
- Further reduction is possible, by optimizing the peripherals

Power Consumption:

- Similar read/write power for same performance
- Less power to retain data (496 → 54 pW/bits), because refresh power is less compared to SRAM cell leakage
- TSV power cost can be contained



3D: Partnering for Cost Effective Research

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