nano.grain

Nanofabrics for reconfigurable computing cores

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Outline

- Some technology fabric considerations
- Logic cells
  - Reconfigurable logic cells and design methods
- Interconnect strategies
  - Matrix topologies
  - Island-style architecture
  - Metrics and comparisons
- Conclusions

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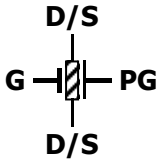
Explaining the jargon

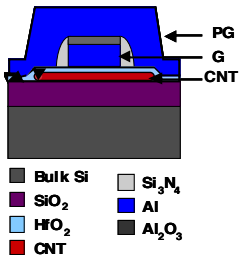
- nanoscale computing fabric (nanoFabric):
  - *nanoFabric*: an array of connected nanoscale logic blocks (nanoBlocks)
  - *nanoBlock*: a circuit block containing programmable devices to compute boolean logic functions and means to route data
- usually hybrid approach (silicon die, or CMOS compatible):
  - bottom-up structure: chemical self-assembly for dense and regular arrangement of elements
  - top-down structure: conventional process options for interconnect or for computation
  - and memory …

Double-gate ambipolarity

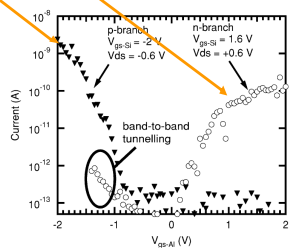
- In DG-CNTFETS, the I_d-V_g characteristic demonstrates ambipolarity



G	PG	state
+V	+V	on (n)
-V	+V	off (n)
+V	-V	off (p)
-V	-V	on (p)
X	0	off (n/p)

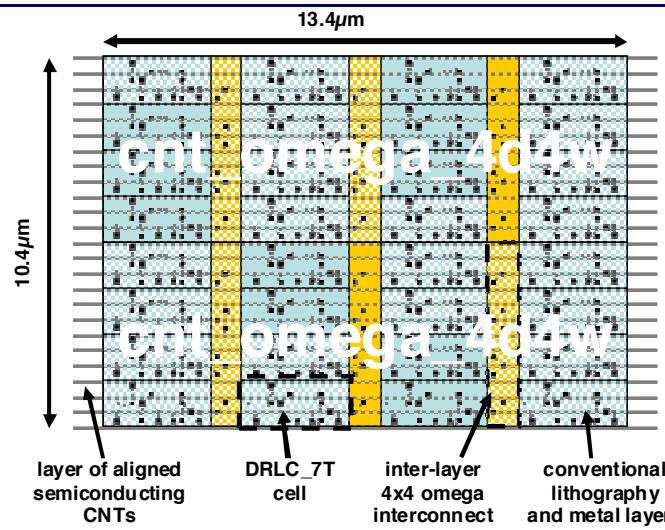


Y.-M. Lin *et al.*, *IEEE Trans. Nanotechnology*, 4(5),2005



- Verilog-A model developed (IMS)
- Reduced-complexity logic cells
- Ultra fine-grain reconfigurable logic cells

Hybrid technology



- "Selective Growth of Well-Aligned Semiconducting Single-Walled Carbon Nanotubes", L. Ding et al., *Nano Lett.*, 9(2), 800 (2009)
- "Monolithic integration of CMOS VLSI and carbon nanotubes for hybrid nanotechnology applications", D. Akinwande et al., *IEEE Trans. Nanotechnology*, 7(5), 636 (2008)

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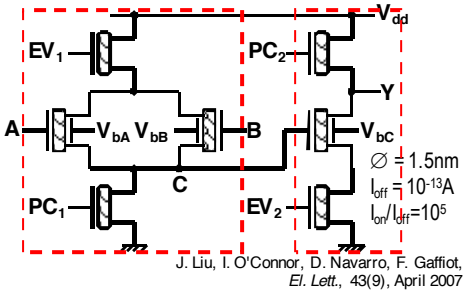
Reconfigurable logic cell CNT-DR7T

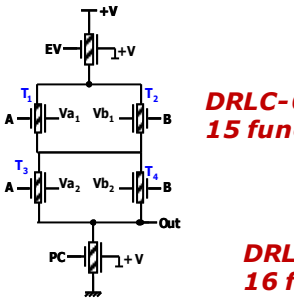


J. Liu, I. O'Connor, D. Navarro, F. Gaffiot, *El. Lett.*, 43(9), April 2007

V_{bgA}	V_{bgB}	V_{bgC}	Y
+V	+V	+V	$\overline{A+B}$
+V	+V	-V	A+B
+V	-V	+V	$\overline{A}.B$
+V	-V	-V	$A+\overline{B}$
-V	+V	+V	$A.\overline{B}$
-V	+V	-V	$\overline{A+B}$
-V	-V	+V	A.B
-V	-V	-V	$\overline{A.B}$
+V	0	+V	$\overline{A}$
+V	0	-V	A
0	+V	+V	$\overline{B}$
0	+V	-V	B
0	0	0	1
0	0	-V	0

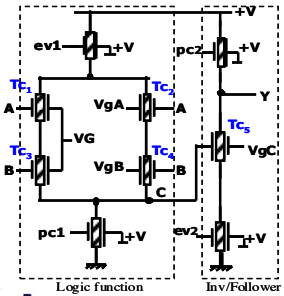
- boolean data inputs A and B, data output Y {0,+V)
- four-phase non-overlapping clock signals PC_1, PC_2, EV_1, EV_2 {0,+V)
- ternary configuration inputs V_{bgA}, V_{bgB}, V_{bgC} {-V,0,+V)

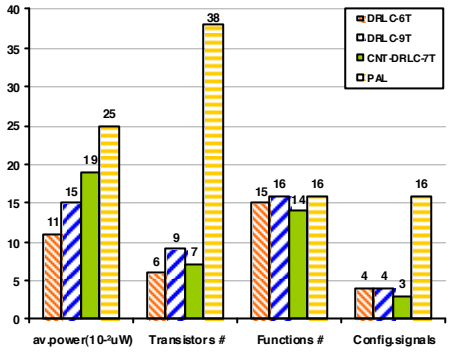
Towards complete operator sets



DRLC-6T
15 functions

DRLC-9T
16 functions





- 1.5X-2X decrease in power consumption
- more functions, fewer transistors, one extra configuration signal

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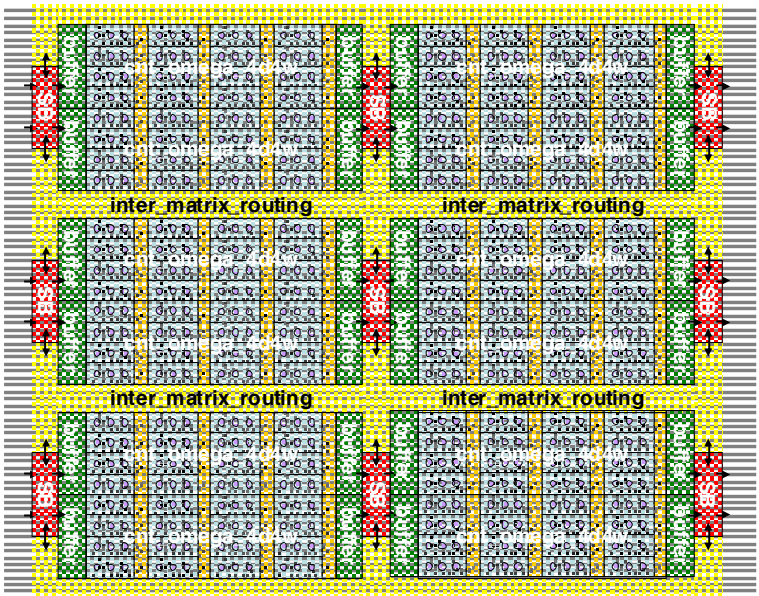
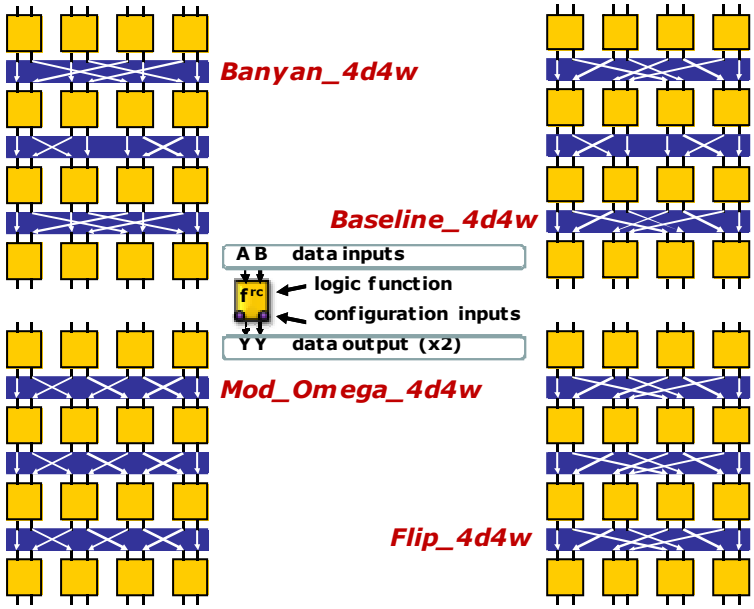
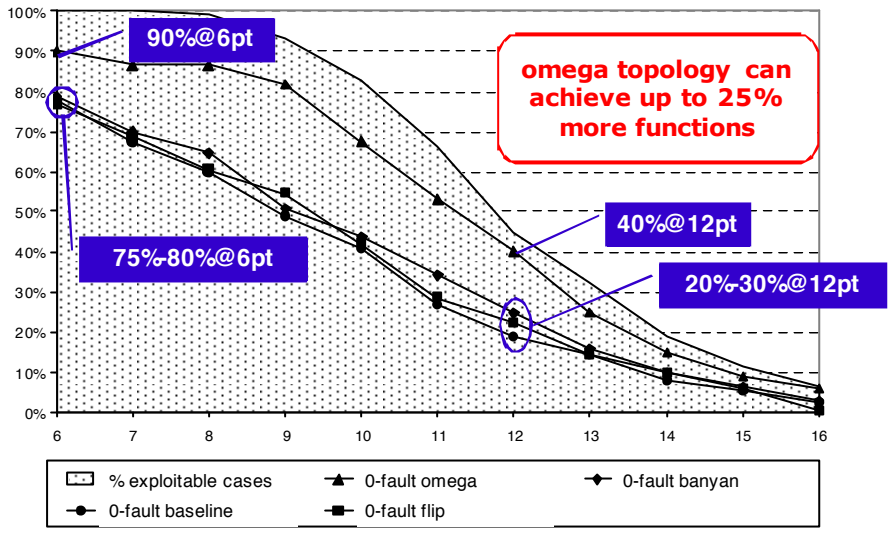
Physical view: clusters of matrices



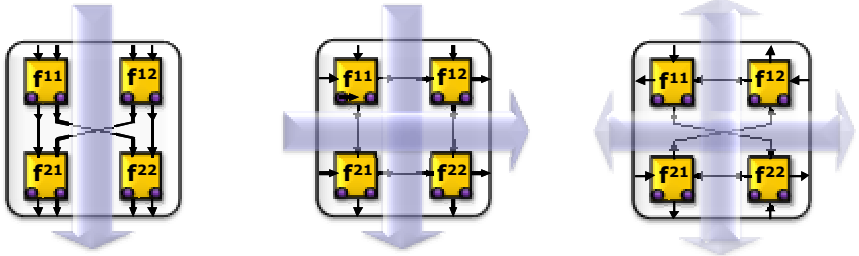
Directed matrix interconnect topologies



Mapping success rate for matrices



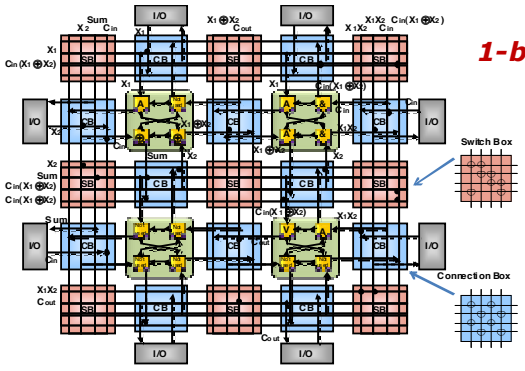
Towards undirected topologies



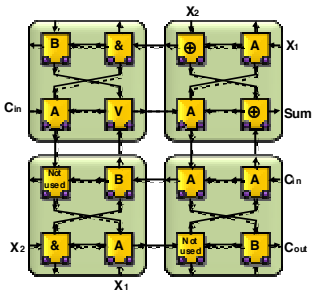
Banyan *Systolic array* *Cross-cap*

Metrics	Banyan	Systolic array	Cross-cap
Max. I/O data width / side	--	-	+
Intra-matrix connectivity	-	-	+
Total wire length	$2a+2\sqrt{2}a(w-1)$	$wa+2a(w-1)$	$2a+2\sqrt{2}a(w-1)$
Max. primary I/O path length	$a(\sqrt{2}+1)$	$wa+2a(w-1)$	$2a+2\sqrt{2}a(w-1)$
Av. mapping success rate (2x2)	61%	58%	66%

When to move to island-style?



1-bit FA application



Island-style *Cell-matrix*

Metrics	Island-style	Cell matrix
No. transistors involved in mapping, *T*	258	375
% mapped matrices in a cluster	75	100
No. of switches added to connect matrices	168	0

Wrap-up

- Logic with ambipolar DG-CNTFETS:
  - complete operator set dynamic-logic reconfigurable cells with low transistor count and power consumption
- Interconnect strategies:
  - directed matrix interconnect topology exploration
  - cross-cap topology proposed to relieve latency and data-directivity issues
  - matrices within islands allow efficient packing
  - routing between islands to be explored …