MPSOC Synthesis: Combining NOC Synthesis with Multiobjective Design Space Exploration on Large Scale Emulator

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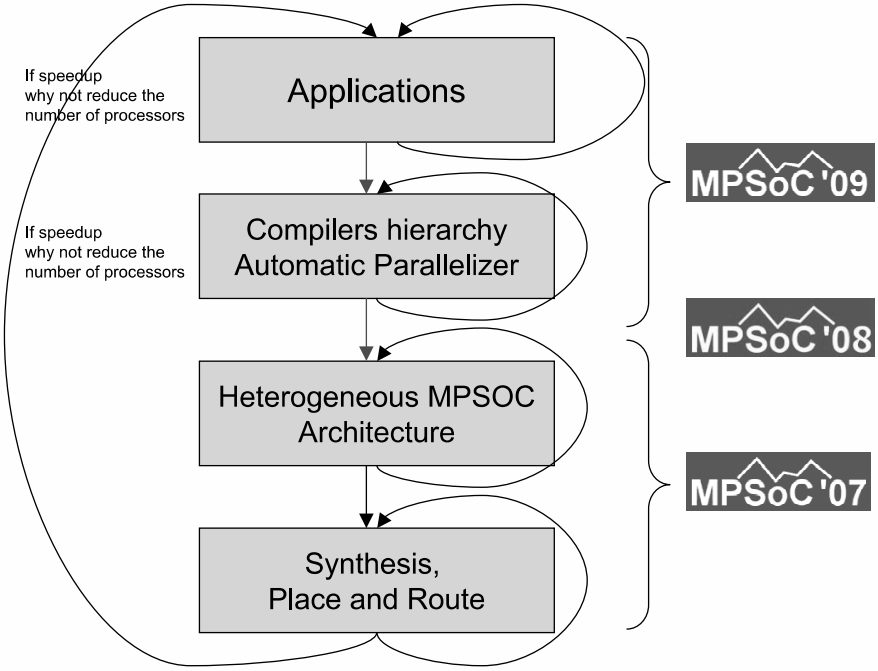
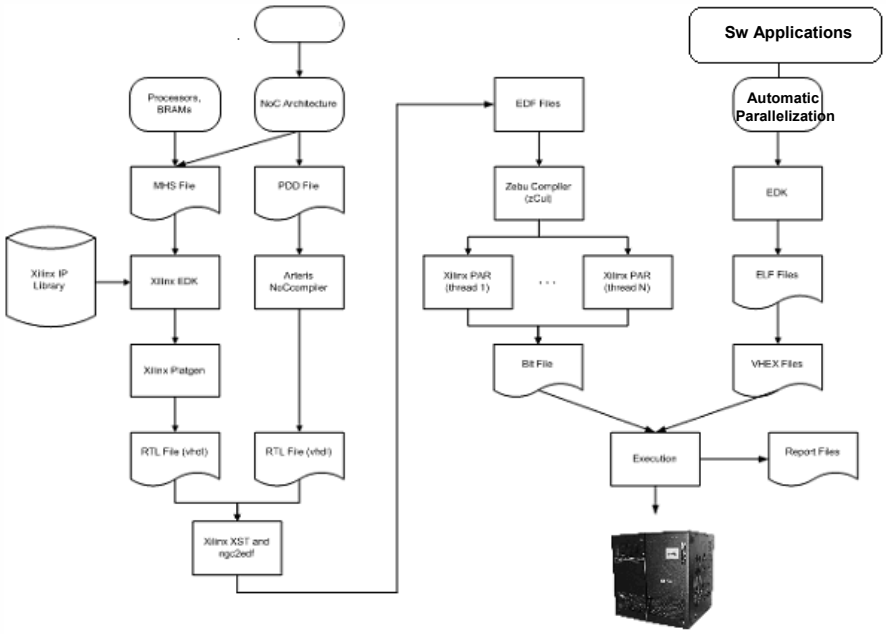
Outline

1. Design Space Exploration
2. NOC Synthesis
3. Design Implementation
4. Conclusion

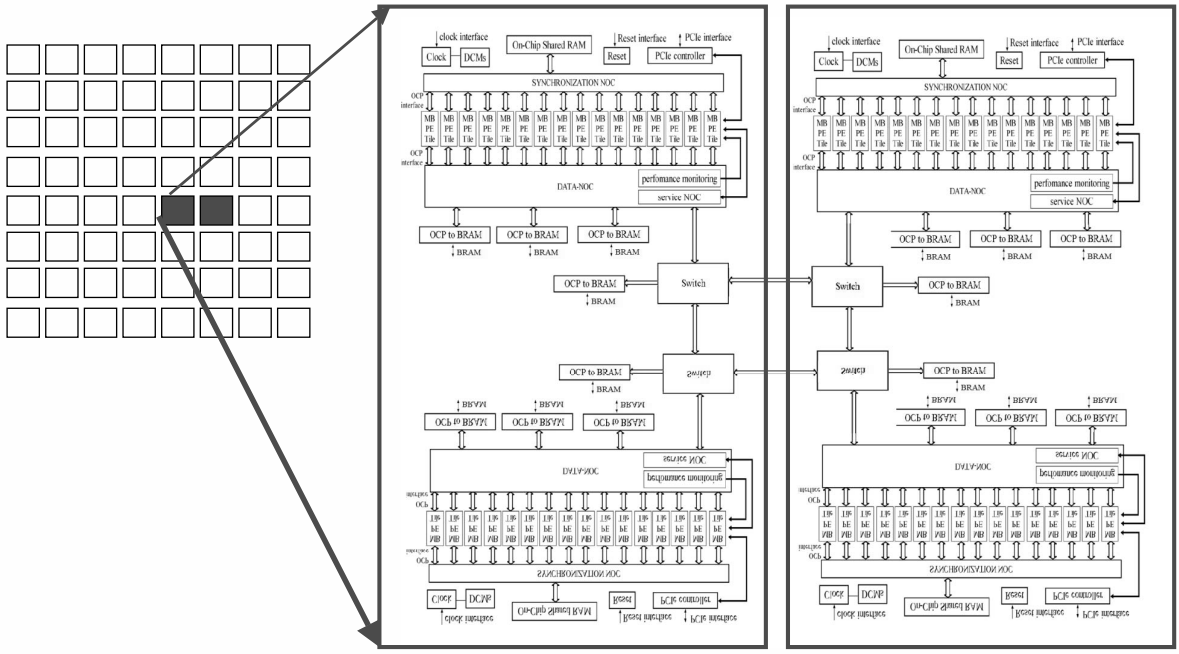
Very Large Scale DSE



2048-PE Automatic Design Flow



2048 PE NOC Based MPSOC



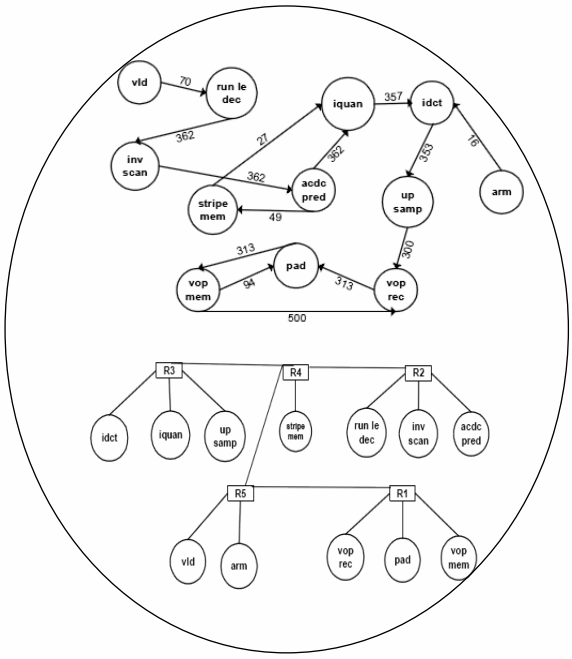
Very Large Scale Emulator

Eve ZeBu Server
Virtex-5 LX330

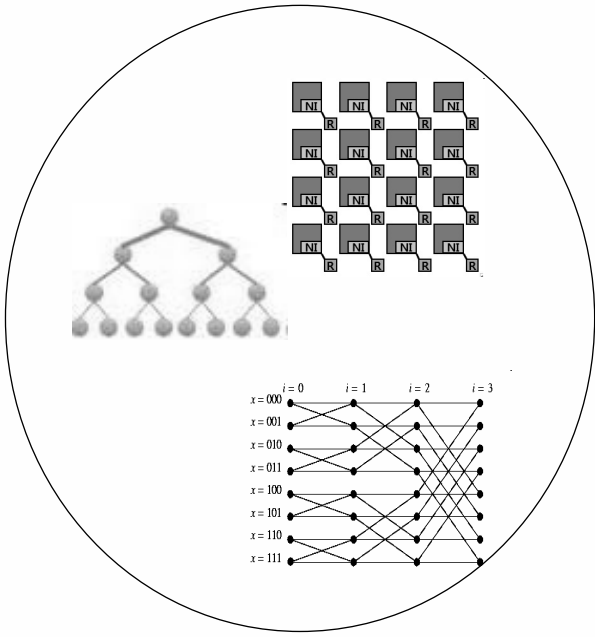
Operating Mode	Performance Range
Max capacity in ASIC gates	1 G (max capacity)
Co-emulation with commercial HDL simulator	5k - 100kHz
Co-emulation with signal-level C/C++/SystemC	100k - 500kHz
Co-emulation with transaction-level C/C++/SystemC/SystemVerilog	200k - 20MHz
Test vectors	100k - 500kHz
Emulation with synthesizable test bench	2M - 50MHz
In-circuit emulation, connected to target system	2M - 50MHz

Introduction (1/2)

NoC architectures can be designed as regular or application specific topologies



application specific NoC topologies



regular NoC topologies

Introduction (2/2)

- As a motivating example, the comparison of two different NoC topologies for a video processor SoC with 42 cores is presented in Table 1
- The first topology is a mesh, while the second is a custom topology generated using the methodology presented in [1].

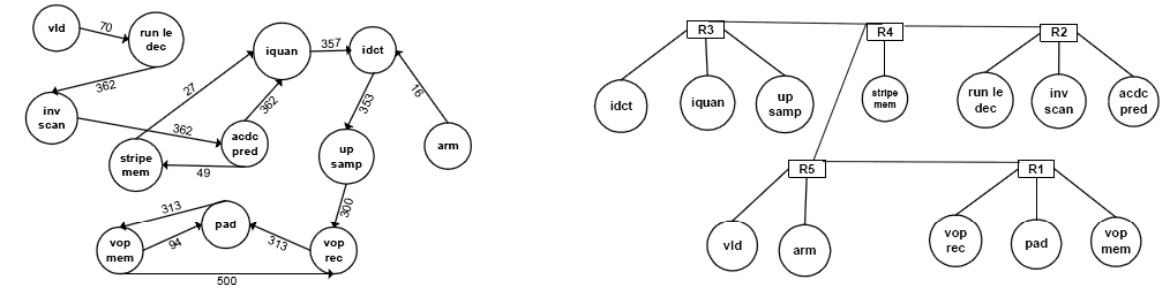
Table 1: Topology Comparisons

Parameter	Mesh	Application-specific
Power (mW)	301.78	79.64
Hop-Count	2.58	1.67
Total wire-length (mm)	185.72	145.37
Design Area (mm^2)	51.0	47.68

[1] Srinivasan Murali and al, '' **Designing Application-Specific Networks on Chips with Floorplan Information '' ICCAD '06 Proceedings of the 2006 IEEE/ACM international conference on Computer-aided design**

NoC Synthesis Definition

- The NoC synthesis can be defined as the generation of a custom network architecture optimized to the needs of the application



[1] **Figure 2 : The core flow graph (CFG) and the final irregular topology of application**

Single Opbjective Optimization :

Ex :Area or performance

Multiobjective Optimization :

Ex:Area and performance

[1] **Yilmaz Ar and al, ''TopGen: A New Algorithm for Automatic Topology Generation for Network on Chip Architectures to Reduce Power Consumption '', Application for Information and Communication Technologies , 2009, AICT 2009**

Related Work

1. Srinivasan and al. presents a MILP(Mixed Integer Linear Programming) based NoC synthesis solver with objective of minimizing power consumption subject to performance constraints in [1], and they uses Genetic Algorithm to improve synthesis run time of large scale system with slightly more power consumption [2].

2. Shijun Lin and al. present a hierarchical cluster-based NoC synthesis method focusing on power optimization as single objective[3]

3. Murali and al, present a complete NoC design flow in [4]. During the NoC synthesis process, they focus on power optimization while performance is not targeted.

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Related Work

MPSoC'11

All these related NoC synthesis technologies are not multi-objective optimization based

- The only multi-objective NoC synthesis based on simulation is presented in [5]; but still it's for regular NoC mapping.

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NSGAII Based Multi-Objective NoC Synthesis

MPSoC'11

The proposed method aims at multi-objective multistage topology NoC synthesis for specific applications using Multi-Objective Evolutionary Algorithm (MOEA). In this case, NSGAII[1] is used.

[1] Deb, K., S. Agrawal, Amrit Pratap and T. Meyarivan (2000), A fast elitist non – dominated sorting genetic algorithm for multi-objective optimization: NSGA II. In M. S. et al. (Ed), *Parallel Problem Solving From Nature – PPSN VI*, Berlin, 849 – 858. Springer

- Directed core graph G (V_m, V_s, E) with each vertex v_m Vm representing a master core (processing element), v_s V_s representing a slave core (memory unit) and the directed edge (v_m, v_s), denoted as $e_{m,s}$ E, representing the communication between the master core v_m and slave core v_s .

- The weight of the edge $e_{i,j}$, denoted by $w(e_{i,j})$, represents the bandwidth in MB/s of the communication from v_i to v_j. And $d(e_{i,j})$ represents the latency constraint in ns

- H_i and H_o denote the maximum input and output port numbers of switch, and Ω denotes the peak input and output bandwidth that switch can support on any one port

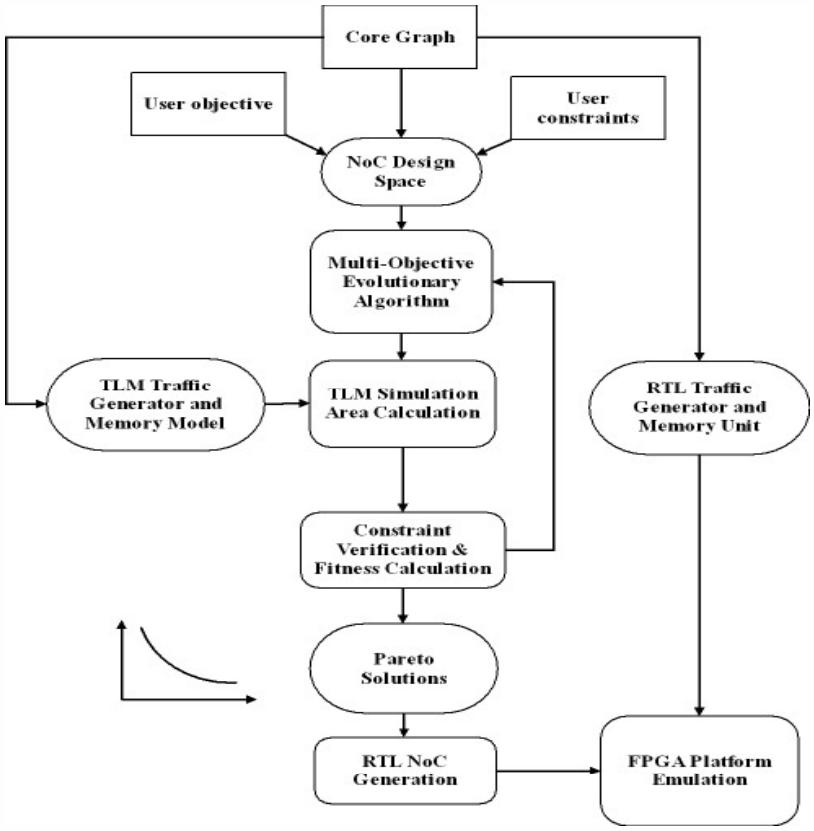
- $A_{i,o}$ and $F_{i,o}$ denote the area and the frequency of the switch with *i* input ports and *o* output ports.

The NoC synthesis problem is to supply a suite of NoC configurations (interconnections and routings) as Pareto solutions for the multi -objective NoC design, so that :

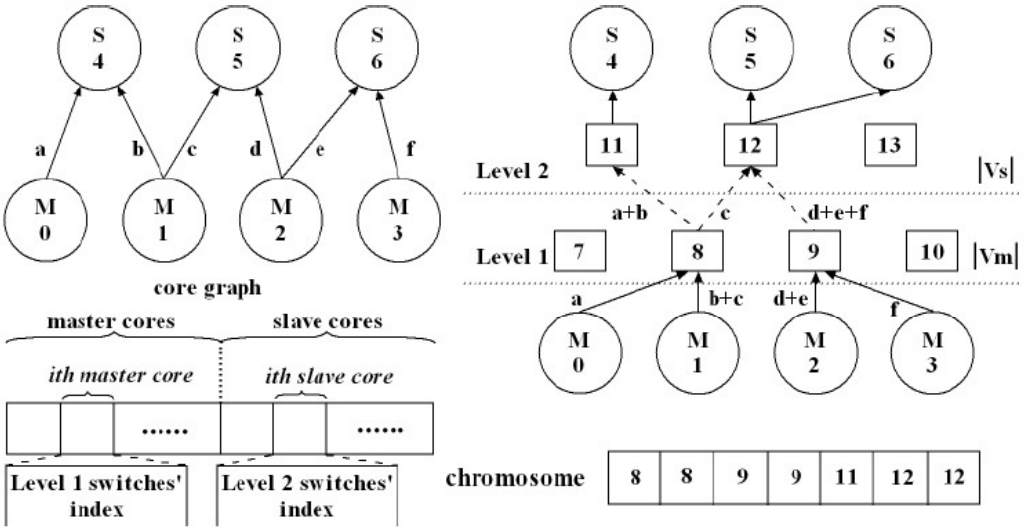
- For each $e_{i,j}$ E, there exists a routing in the NoC that satisfiers the bandwidth $w(e_{i,j})$ and latency $d(e_{i,j})$.

- The bandwidth constraint Ω of each switch is satisfied.

Multi-Objective NoC Synthesis & FPGA Prototyping Flow



Solution Representation and Routing Construction of Multi-stage NoC



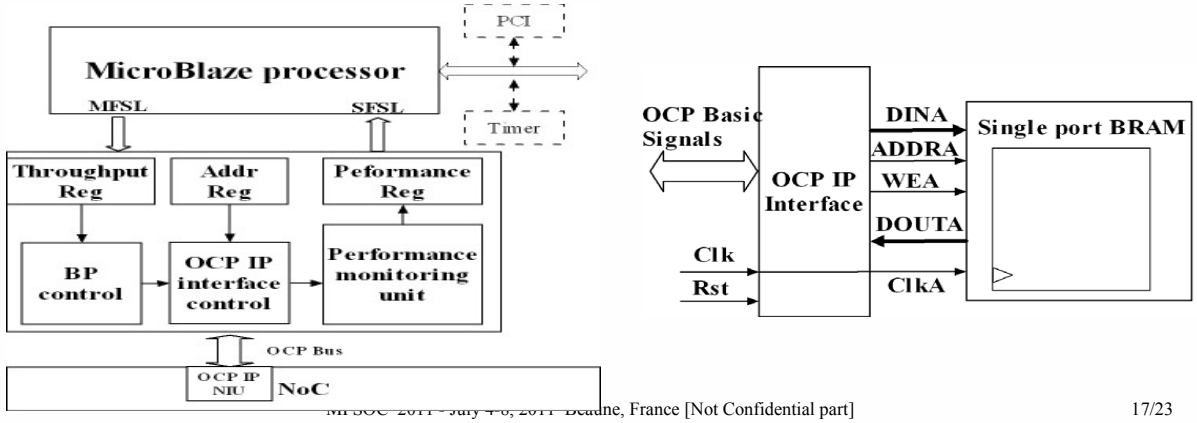
The input of multi-objective genetic evolutionary algorithm is the chromosome, which represents the topology and configuration of NoC architecture

Traffic Generator and Memories

- Traffic generator and memory models are generated according to the core graph for TLM simulation and FPGA emulation.

- Frequency, transaction address and time are all considered in the traffic generator and memory model to perform a fast SystemC TLM simulation.

- TLM and RTL models with same configurations

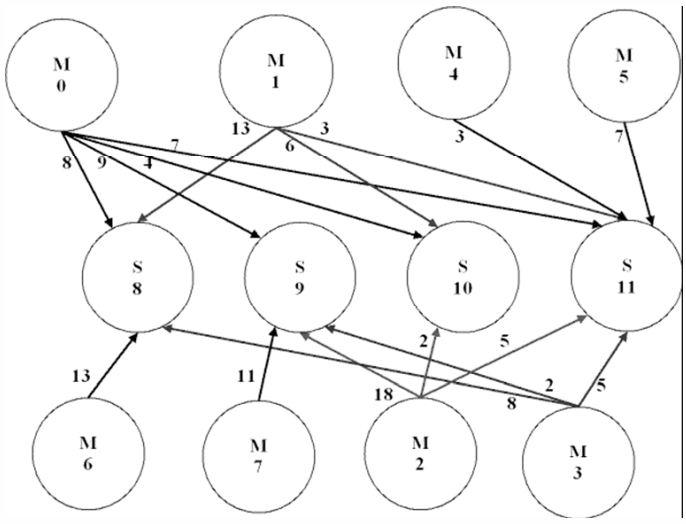


Experimental Results : Core graph Benchmarks

- The multimedia MPEG4 benchmark application and also a general core graph are used in the experiment

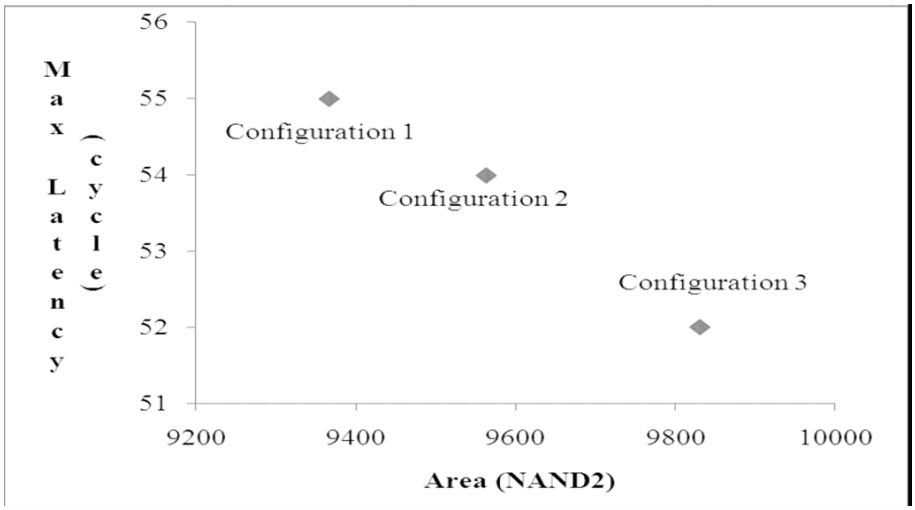
NSGA-II parameters

Population size	200
Cross Over Probability	0.9
Mutation Probability	0.1



General 8 Masters and 4 Slaves core graph

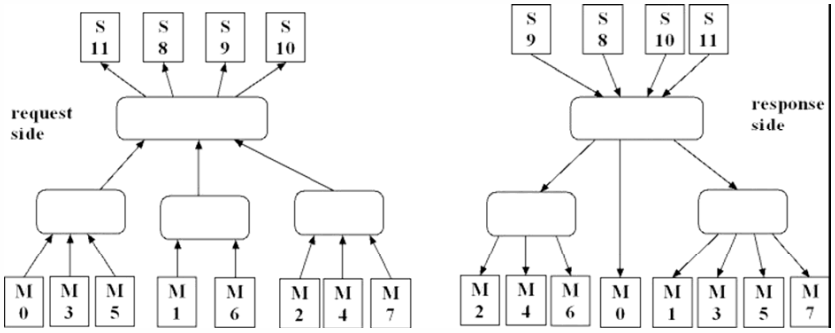
Experimental Results : Results and Discussion



	TLM simulation			FPGA implementation		
	Area (NAND2)	Area Normalized	Max Latency	Area (Slice)	Area Normalized	Max Latency
1	9366	1	55	3928	1	23
2	9563	1.021	54	3960	1.008	18
3	9831	1.050	52	4014	1.022	17

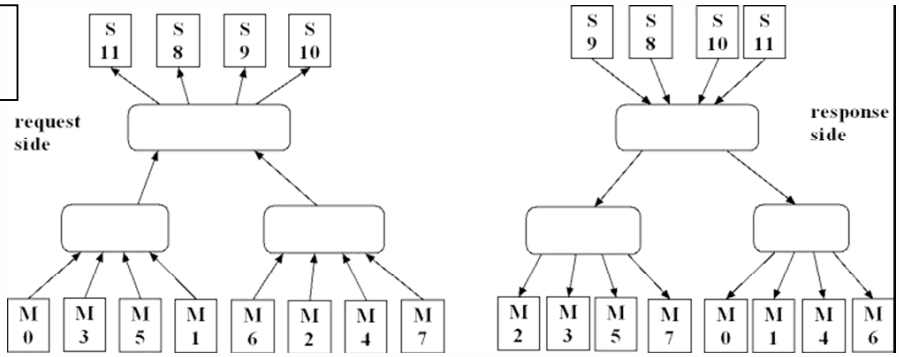
Experimental Results : Results and Discussion

Solution 3 architecture is asymmetrical, as it reduces the latency while it consumes more area



Request and response sides NoC architecture of solution 3

Solution 1 has symmetrical architecture ⇨ less area



Request and response sides NoC architecture of solution 1

Conclusion & Future work

- The multi-objective application specific NoC synthesis problem is defined in this paper, and a novel multi-objective NoC synthesis solver is proposed to design application specific NoC of multi-stage topology.

- The proposed concise and efficient multi-objective solver is used for real and general benchmark applications to supply designers multi-objective Pareto solutions rather than one single objective solution subset

- a bridge from high level model to FPGA executionfor accurate NoC design.

Future work:

- Add power consumption as design objective
- Extend the method to other NoC topology.

This work is the work of the full Embedded Systems Group

Thank you for attention.
Questions ?

We wish to thank EVE and Arteris

for their excellent support.