TOSHIBA
Leading Innovation

Heterogeneous Multi & Many Core Processors for Multimedia Applications

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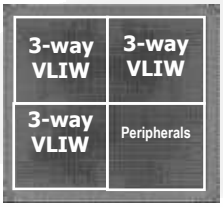
Toshiba Corporation

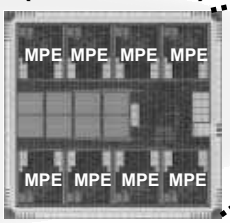
Toshiba's MPSoCs

Multi-core (CICC '03)



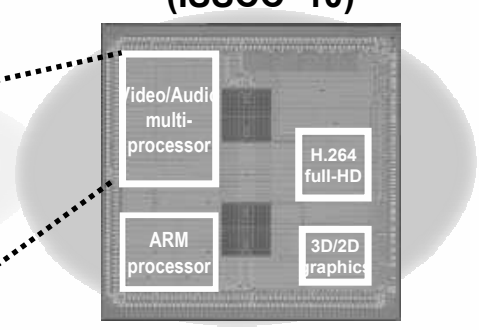
- **Three 3-way VLIW processors based on configurable processor**
- **0.13μm CMOS**
- **150MHz**

Multi-core (ISSCC '08)



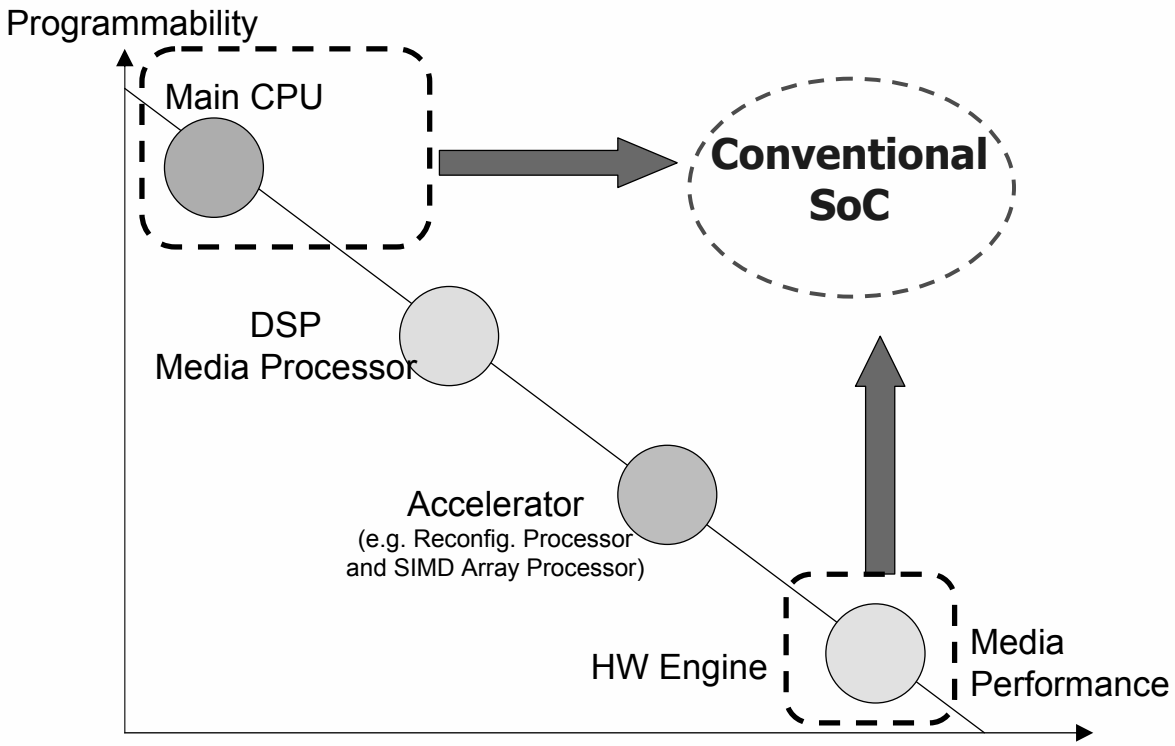
- **Eight 3-way VLIW processors**
- **512KB L2 cache**
- **65nm CMOS**
- **333MHz**

Heterogeneous MPSoC (ISSCC '10)

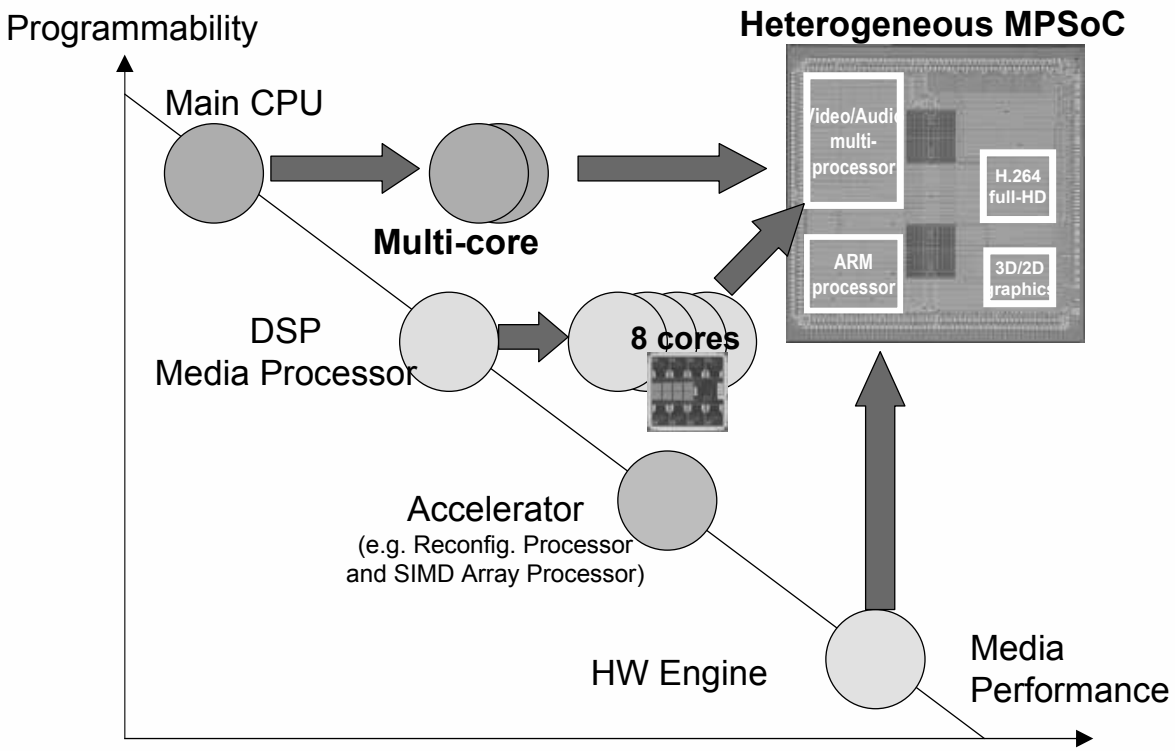


- **Heterogeneous 14 cores**
  - Two ARM cores
  - Eight media engines
  - Four control cores in HW codec and TS i/f
- **CODEC**
  - –H.264 HP 1080i/p HW codec
  - –SW codec up to 720p
- **40nm CMOS**
- **333MHz (A/V multi-core)**

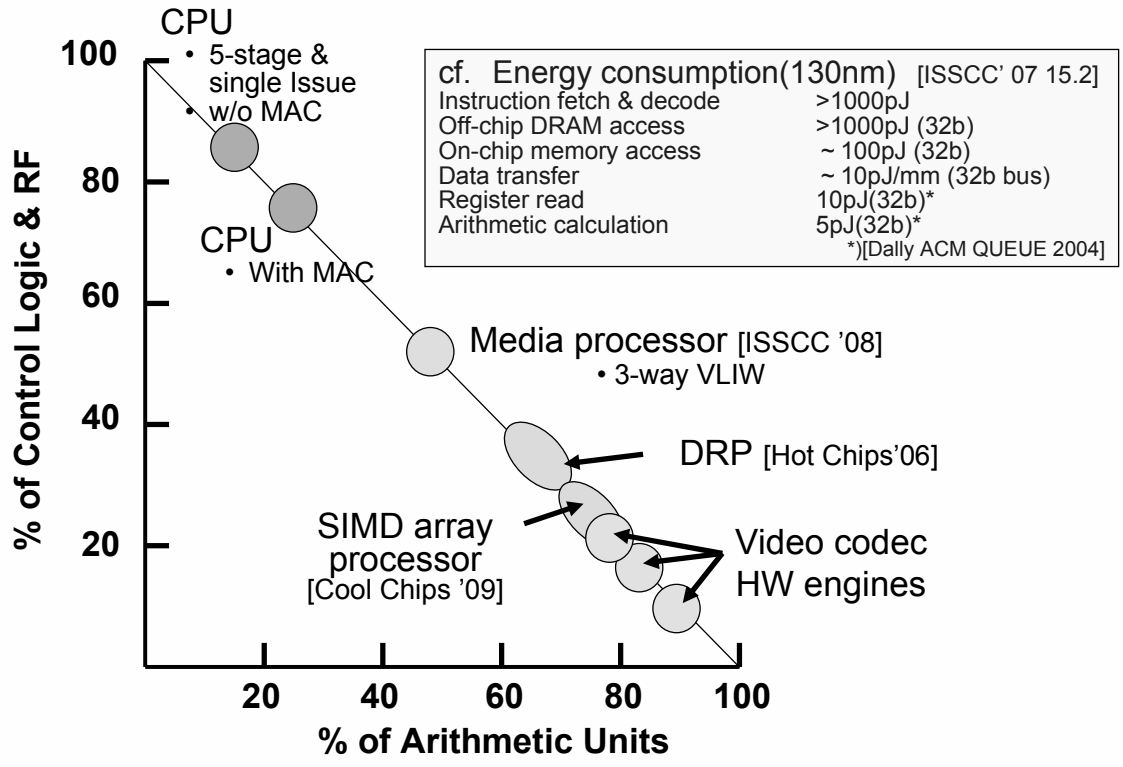
Conventional SoC Architecture



Why Heterogeneous MPSoC?



Gate-count Ratio of Arithmetic Units

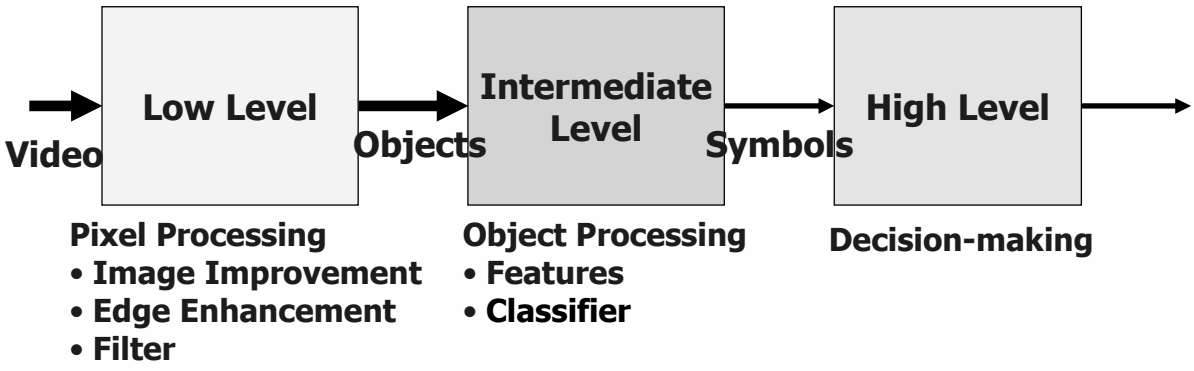


cf. Energy consumption(130nm) [ISSCC' 07 15.2]

Instruction fetch & decode	>1000pJ
Off-chip DRAM access	>1000pJ (32b)
On-chip memory access	~ 100pJ (32b)
Data transfer	~ 10pJ/mm (32b bus)
Register read	10pJ(32b)*
Arithmetic calculation	5pJ(32b)*

*)[Dally ACM QUEUE 2004]

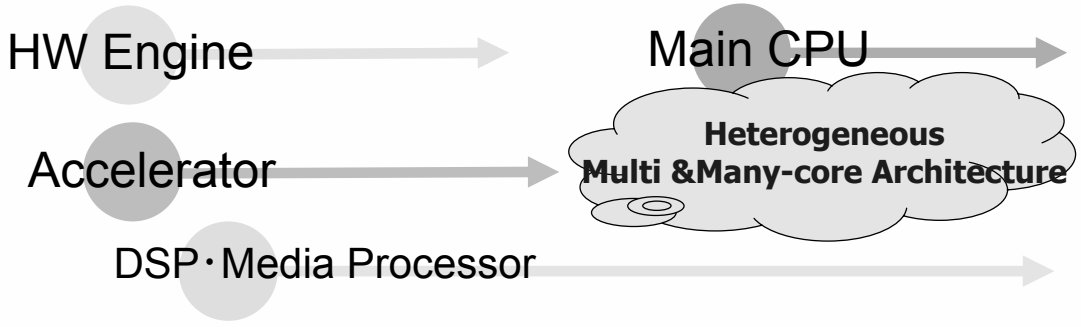
Three levels of Image Recognition Processing



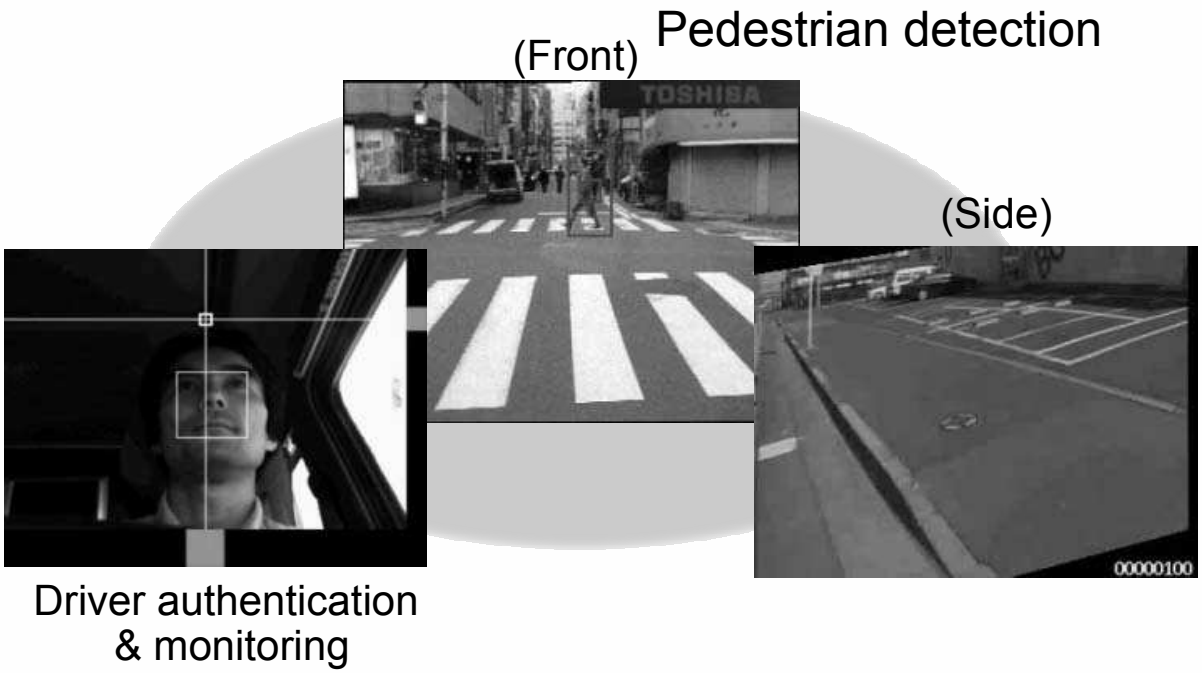
Pixel Processing
- **Image Improvement**
- **Edge Enhancement**
- **Filter**

Object Processing
- **Features**
- **Classifier**

Decision-making

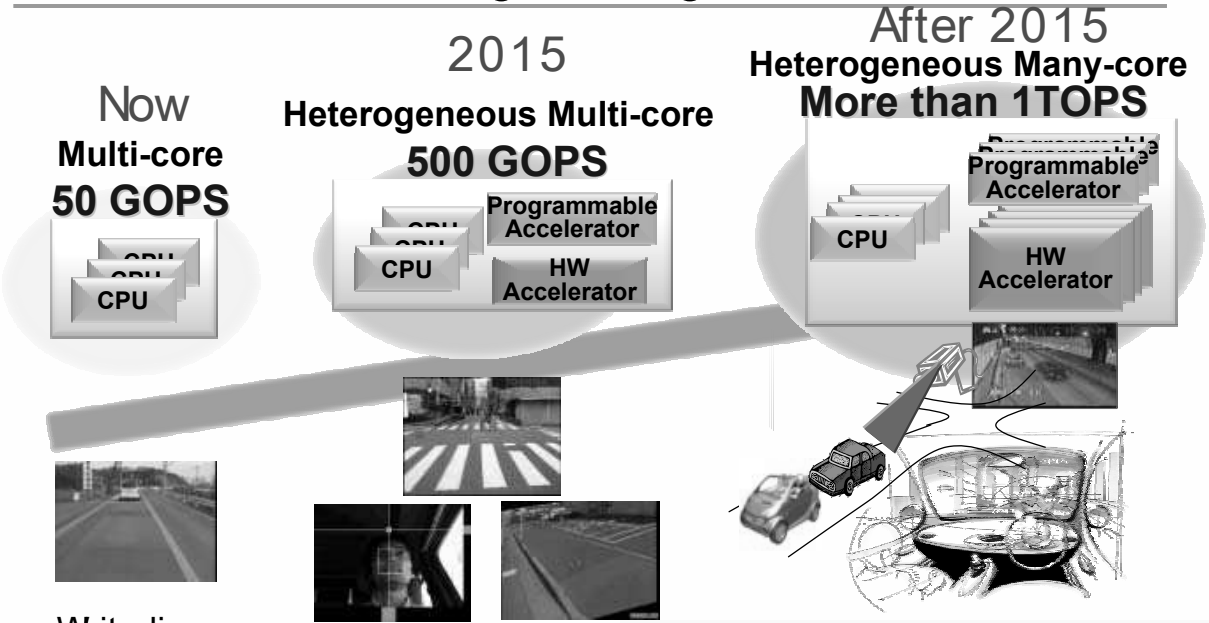


Evolution of Recognition Technology for Automotive



Parallel execution of multiple applications

Future Trends of Image Recognition SoCs

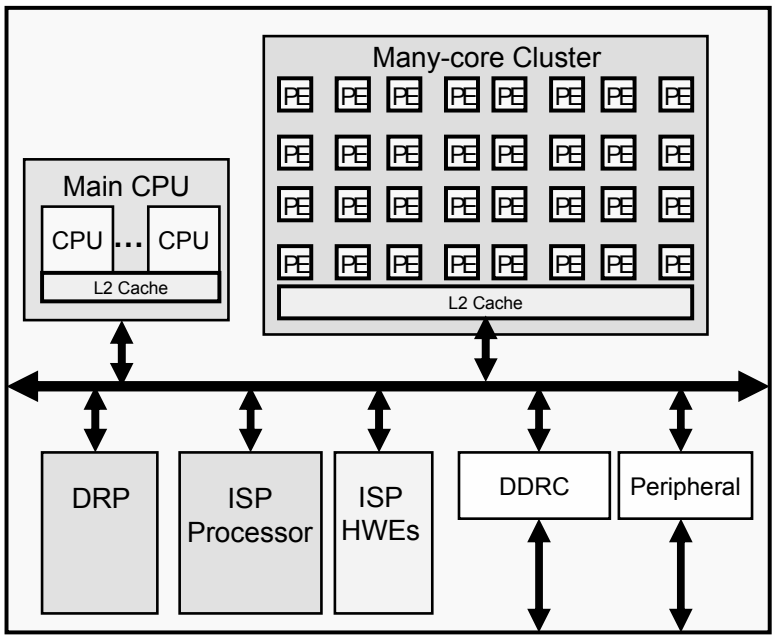


White line detection

Parallel execution of multiple applications

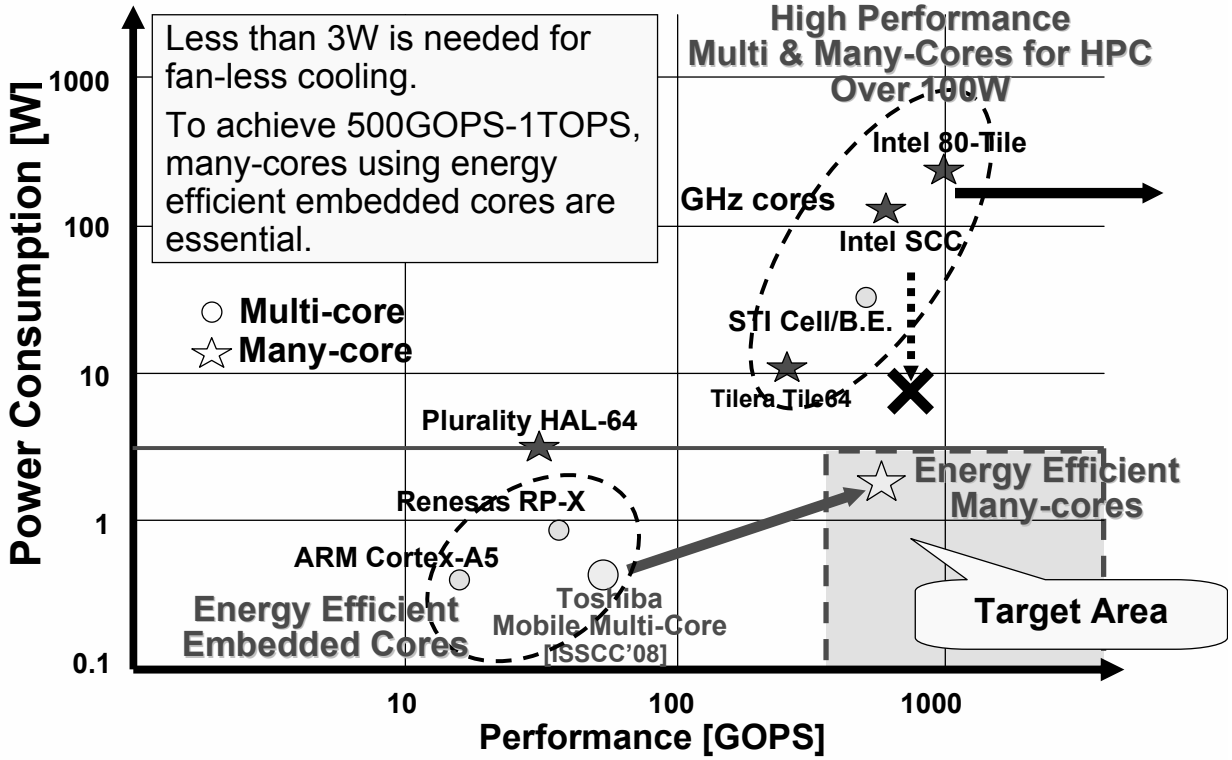
Automatic self- driving
Cooperation with infrastructure and cloud servers

Heterogeneous Many-core Architecture



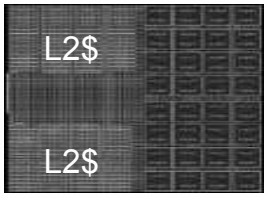
- **Main CPU**
  - Symmetric Multi-core (e.g. ARM)
- **Media processor**
  - Many-core based on energy efficient media processors
- **Accelerators**
  - Dynamically reconfigurable processor
  - SIMD array processor [Cool Chips '09]
- **Hardware Engines**
  - for ISP (Image Signal Processing) and image recognition

Energy Efficient Many-cores for Embedded Applications



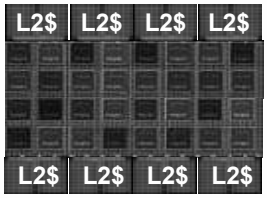
Evaluation of Many-core for Media Processing

- **32-core P&R evaluation results at 65nm**

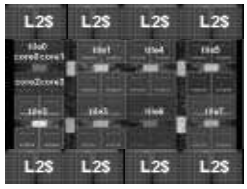


X-bar (87.4mm2)

Torus (83.5mm2)



Mesh(81.9mm2)



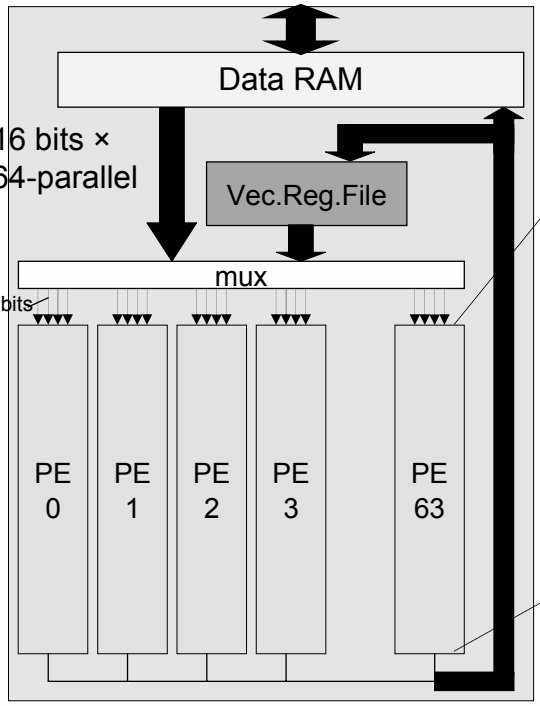
Fat-Tree(71.9mm2)

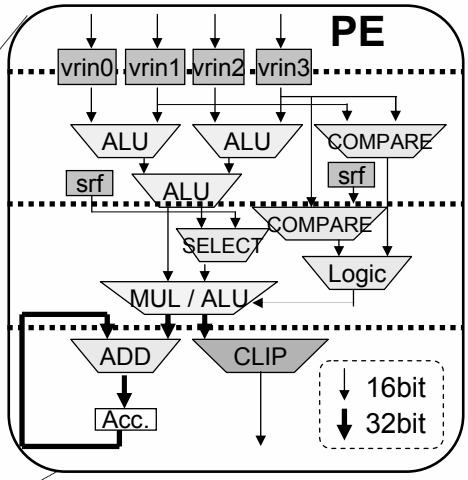
32 cores	X-bar	Mesh	Torus	Fat-Tree
Area	1	0.94	0.96	0.82
Power*	1	0.72	1.45	0.45
Performance	1	0.94	0.95	0.93

*** Only NoC portion**

Fat-Tree topology is better than others (X-bar, mesh, and torus) in terms of area, power consumption with only 7% performance degradation from X-bar.

SIMD Array Processor for ISP [Cool Chips '09]



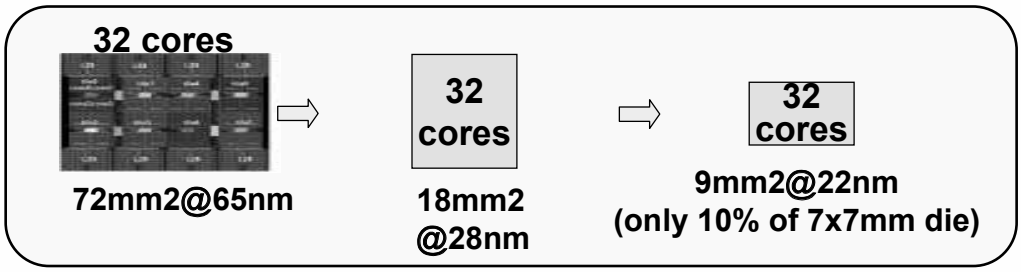


10 arithmetic & logic units
ALU x 3, Comparator x 2, Multiply/ALU, Adder, Logical, Selector, Clip
→ 10 x 64 SIMD = 640 operations
Peak performance: more than 100GOPS@160MHz

5-10x better performance/area efficiency than media processor

Summary

- For embedded application, heterogeneous ***multi-core*** architecture will evolve to heterogeneous ***many-core*** to achieve good power-consumption and performance efficiency.
- Small enough to be integrated in cost sensitive SoC in 22nm.



- Accelerators such as SIMD array processor and DRP will used for specific domain of processing (e.g. ISP, bit-stream processing).