- HOW TECHNOLOGY R&D LEADERSHIP
- BRINGS A COMPETITIVE ADVANTAGE
- FOR MULTIMEDIA CONVERGENCE

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Technology Platform Segmentation

High Performance "HP"	Computers
General Purpose "G"	Computer Peripherals
Low power "LP"	Communication Infrastructure
Analog MS/RF/BCD /Derivatives	Consumers
	Wireless
	Automotive
	Industrial
	Multi segment

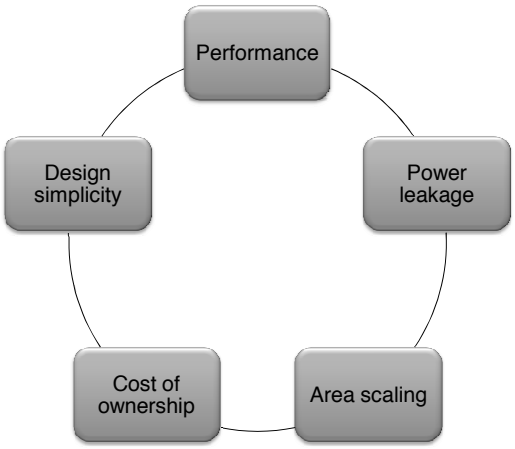
Technology Platform KPIs

High Performance

General Purpose

Low power

Analog MS/RF/BCD /Derivatives



Technology R&D/MFG Leadership Brings

Time-to-Market

- First device tape out in most advanced partner Fab.
- Device volume and yield ramp up thru fast learning technics.

Innovation

- Device performance, power, area scaling.
- Device Add on.
- Cost-of-ownership, design simplicity

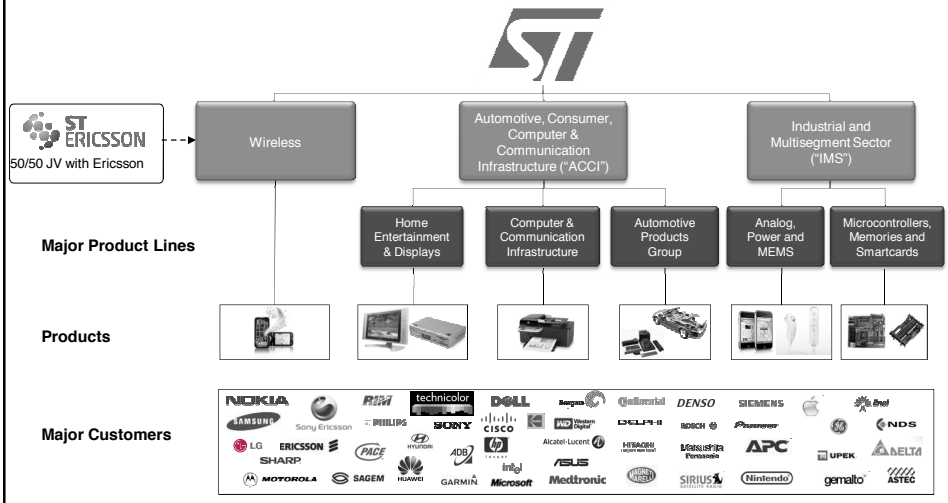
Supply-Chain Multi Sourcing

- Time-to-Market first source
- Second /Alternative source thru Manufacturing Synchronization.

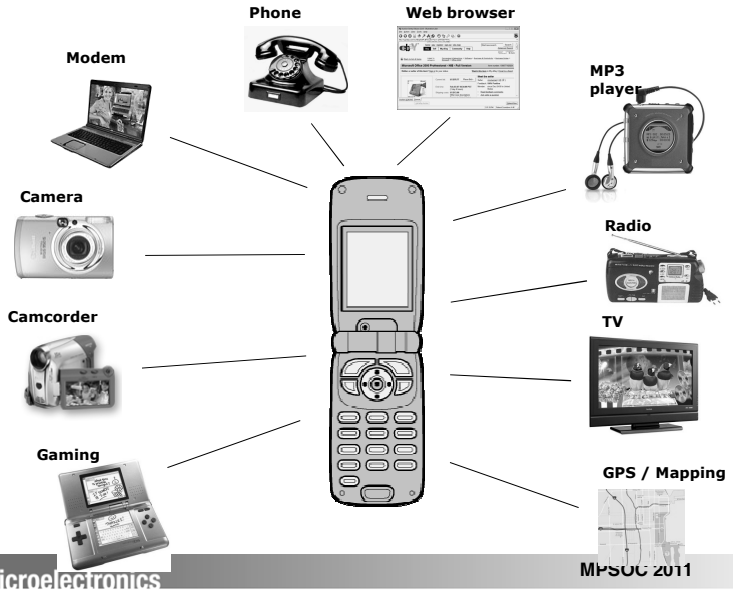
Sustainable Effort

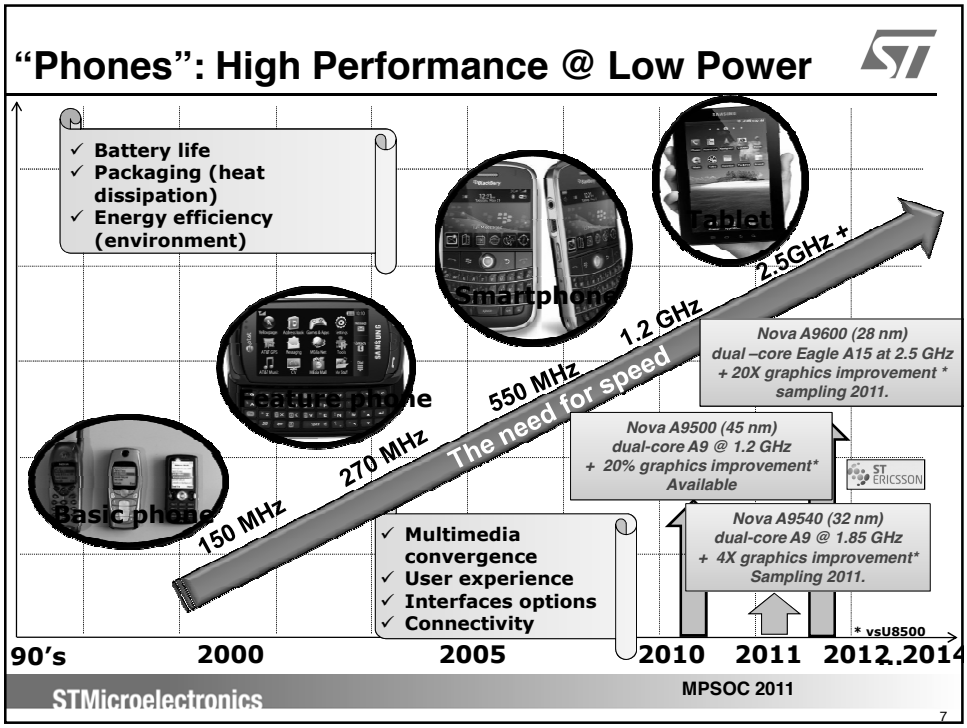
- cooperative model allows leveraged capture of technology innovation with risk mitigation .
- Shared capital/operating expenses thru cooperative/distributed model.

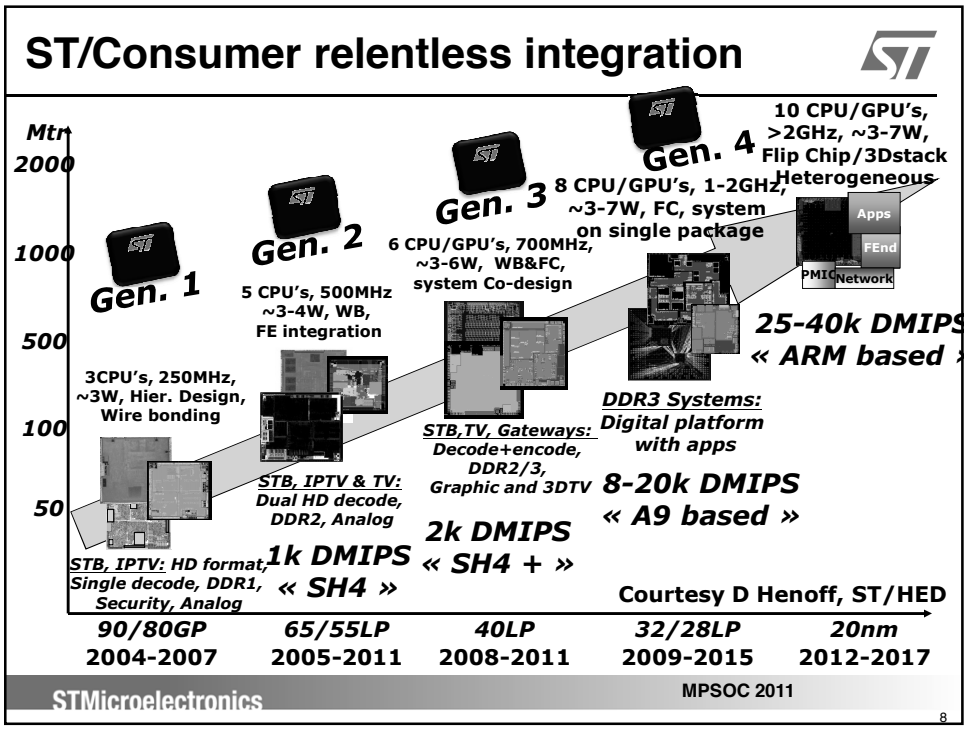
ST Business Segment Overview



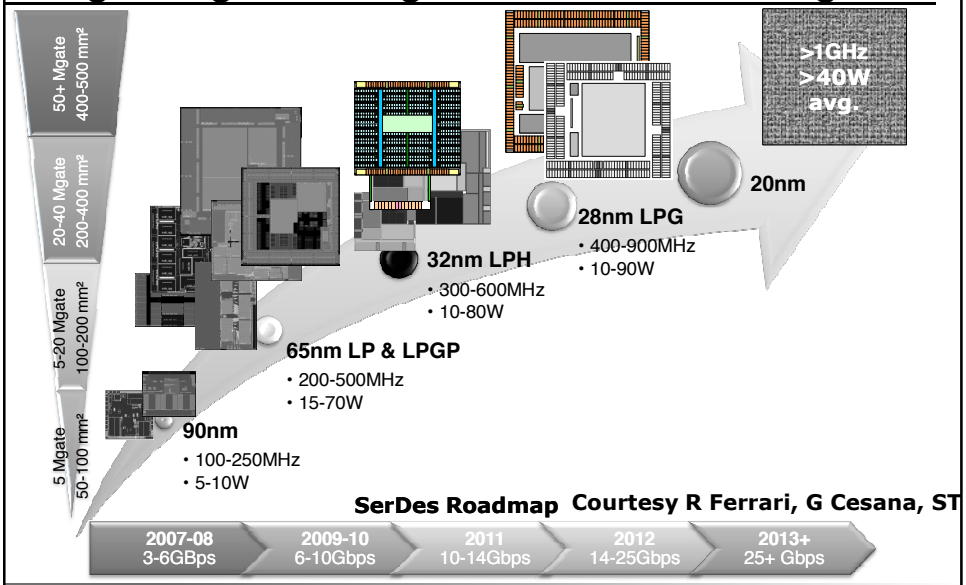
Wireless: multi-purpose Products




"Phones": High Performance @ Low Power
✓ Battery life
✓ Packaging (heat dissipation)
✓ Energy efficiency (environment)
Tablet
Smartphone
Feature phone
Basic phone
150 MHz
270 MHz
550 MHz
1.2 GHz
2.5GHz +
The need for speed
Nova A9600 (28 nm)
dual –core Eagle A15 at 2.5 GHz
+ 20X graphics improvement *
sampling 2011.
Nova A9500 (45 nm)
dual-core A9 @ 1.2 GHz
+ 20% graphics improvement*
Available
ST ERICSSON
Nova A9540 (32 nm)
dual-core A9 @ 1.85 GHz
+ 4X graphics improvement*
Sampling 2011.
✓ Multimedia convergence
✓ User experience
✓ Interfaces options
✓ Connectivity
* vsU8500
90's
2000
2005
2010
2011
2012..2014
STMicroelectronics
MPSOC 2011
7


ST/Consumer relentless integration
Mtr
2000
1000
500
100
50
Gen. 1
3CPU's, 250MHz,
~3W, Hier. Design,
Wire bonding
STB, IPTV: HD format,
Single decode, DDR1,
Security, Analog
1k DMIPS
« SH4 »
Gen. 2
5 CPU's, 500MHz
~3-4W, WB,
FE integration
STB, IPTV & TV:
Dual HD decode,
DDR2, Analog
Gen. 3
6 CPU/GPU's, 700MHz,
~3-6W, WB&FC,
system Co-design
STB,TV, Gateways:
Decode+encode,
DDR2/3,
Graphic and 3DTV
2k DMIPS
« SH4 + »
Gen. 4
8 CPU/GPU's, 1-2GHz,
~3-7W, FC, system
on single package
DDR3 Systems:
Digital platform
with apps
8-20k DMIPS
« A9 based »
10 CPU/GPU's,
>2GHz, ~3-7W,
Flip Chip/3Dstack
Heterogeneous
Apps
FEnd
PMIC
Network
25-40k DMIPS
« ARM based »
Courtesy D Henoff, ST/HED
90/80GP
2004-2007
65/55LP
2005-2011
40LP
2008-2011
32/28LP
2009-2015
20nm
2012-2017
STMicroelectronics
MPSOC 2011
8

ST/ Networking ASICs
A growing SOC integration / Power Challenge



SerDes Roadmap **Courtesy R Ferrari, G Cesana, ST**

2007-08	2009-10	2011	2012	2013+
3-6GBps	6-10Gbps	10-14Gbps	14-25Gbps	25+ Gbps

The ST Technology R&D Model

A Distributed & Cooperative R&D:

- Leveraging best innovation versus :
  - Targeted product
  - Critical decision factor
  - Technology
- Mitigating risks of choice
- Sharing expenses effort

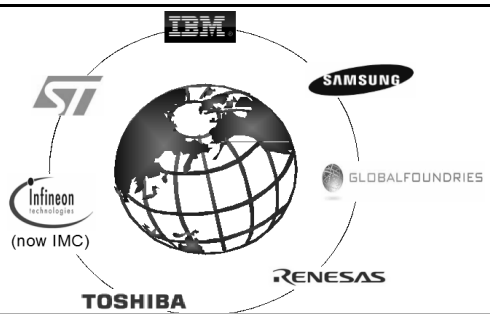
Value-Chain Management : Technology Innovation 1/3

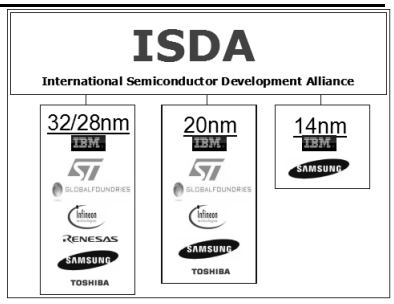
- ***Technology Innovation*** **leveraging**
- **bi / multi parties competence centers:**
  - *Fundamental/ advanced R&D thru joint Academia/Research Institutes Cooperation.*
  - *(CEA LETI being the corner stone.)*
  - *Advanced CMOS thru ISDA ("Pre-T0" in Albany)*

CEA-LETI MINATEC

Univ Albany Nanotech

Value-Chain Management : Technology Operations 2/3

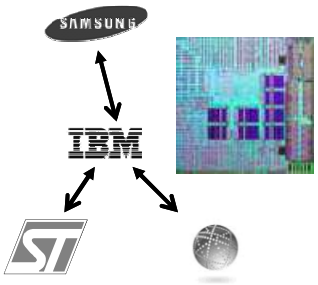




- ***Technology Operations balanced between internal/ext. comp. centers*:**
  - *Advanced CMOS thru* ***ISDA***
  - *CMOS Analog thru* ***internal Cluster*** *of Crolles (France)*
  - *Smart Power/Analog thru* ***internal Cluster*** *of Agrate (Italy)*
  - *Design Enablement thru* ***internal clusters*** *of Agrate/Crolles/Greater Noida (India).*

ISDA MANUFACTURING SYNC 3/3

- **Scope:** Electrical Synchronization of partner fabs to IBM
  - Parametrical equivalence, GDS2-level
- **Contract:** JDA between IBM and partners on 32LP Bulk and 28LP.
- **Timing:** Program started 2H09 (28LP), end DEC2011.



IP circuits Equivalence
Direct validation between ST & foundry, not in Fabsync

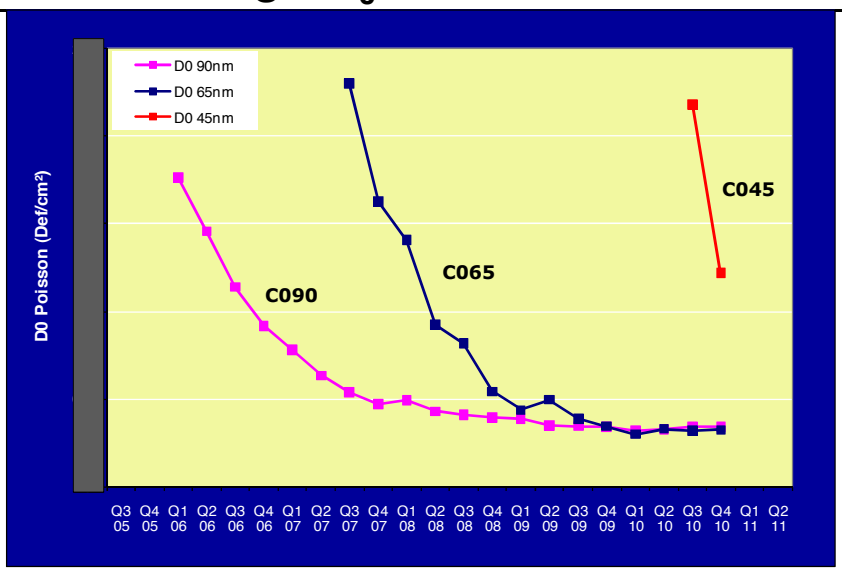
Parametrical Equivalence
Equivalence to model
Model to silicon correlation

In line Cp/Cpk Equivalence
Metrology (SEMCD, Overlay, thin films, material composition) matching

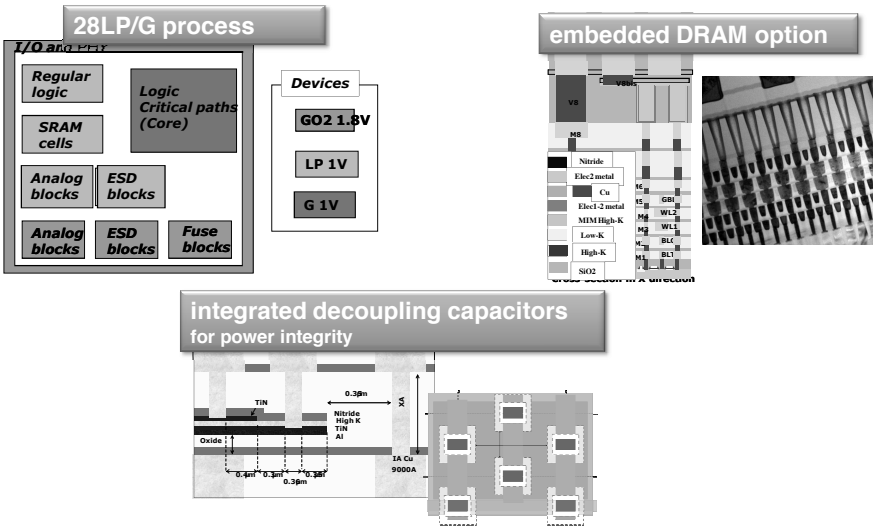
Test vehicle
Common modeling macros
Common electrical monitoring

Process
FEOL & BEOL critical process steps,
Construction Analysis

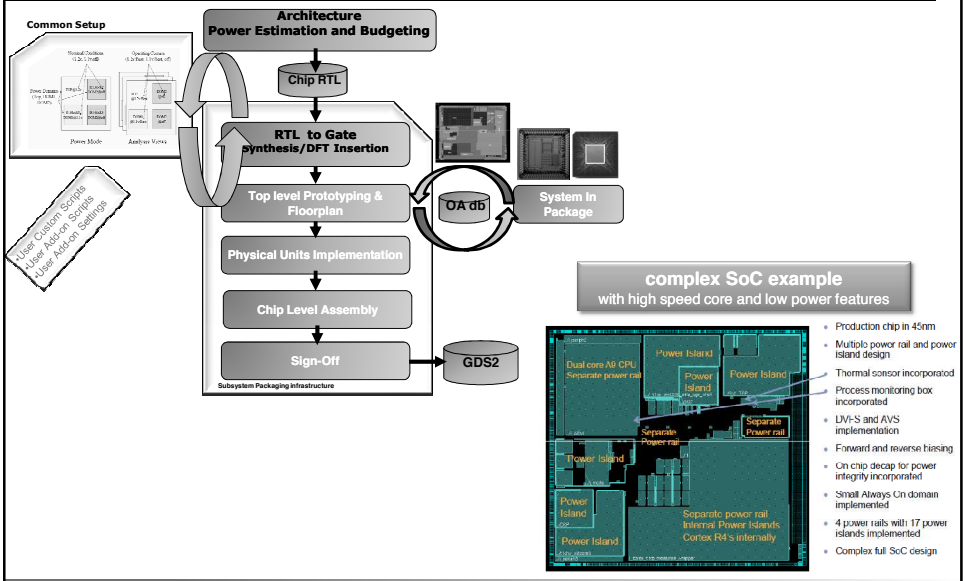
Yield Learning – D_0 Trend – ST/Crolles



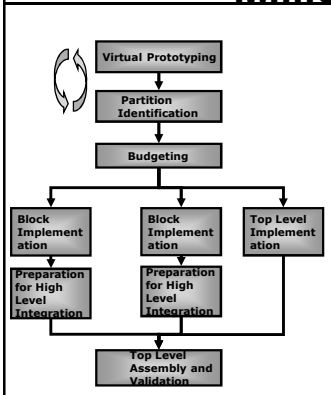
28nm ST Proprietary Process Options



40nm/28nm SOC Design flow: high speed, low power

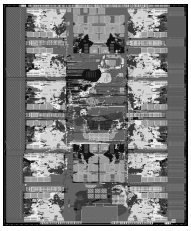


28nm ASIC Design flow: Million Gates Capacity



Hierarchical Flow for Complex Devices

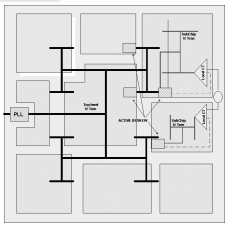
Flexible Abstraction for higher Scalability
Predictable Hierarchical Floorplan Toolkit
Accurate Budgeting
"Correct by Construction" methods



Specialized Clock Distribution Strategy

Hybrid Architecture Support
Mesh, Htree, RC-Matched, CTS

Clock Deskew Components
Variation Tolerant Clock Drivers

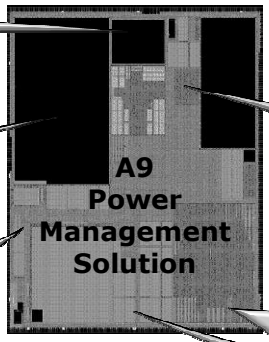


Full Chip Hierarchical Analysis

Design Integrity: Timing, SI/PI
Reliability: EMG

Enabling GHz performance over 500mm2 @ 28/20nm nodes

Enabling performance race on products : STE 32nm 1.5GHz Low Power A9 Core



L1 Cache designed to reach 1.8Ghz

High Density L2 cache designed for 0.6 V Retention

Faster pipelined Memory BIST Architecture

Dedicated algorithms for Memory Test in 32/28nm

High Performance Clock Generator

Fast FF library designed for improving R2R performance in critical paths

Power Switches: Peripheral Switches and Distributed Switches for best Vdrop.

Several IP/Lib Patents Pending

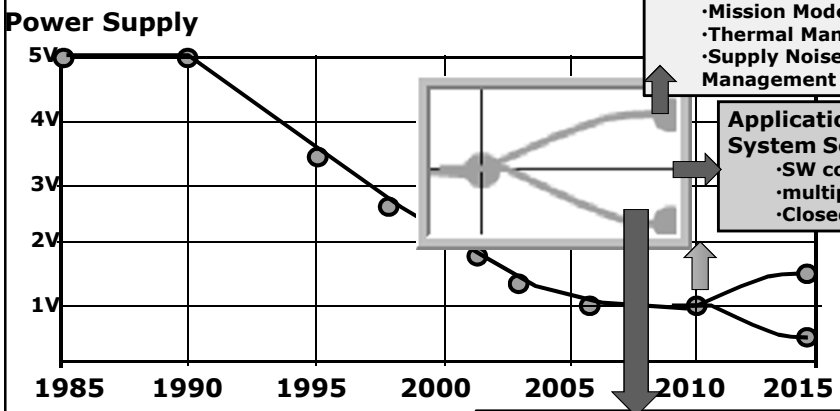
Enabling High speed cores in 28LP

@1.5GHz dual A9 experience

>>1.5GHz quad A15

V_{dd} Scaling and energy efficiency

Scaling driven by process technology (T_{ox})



High Voltage Solutions
- Mission Mode
- Thermal Management
- Supply Noise Management

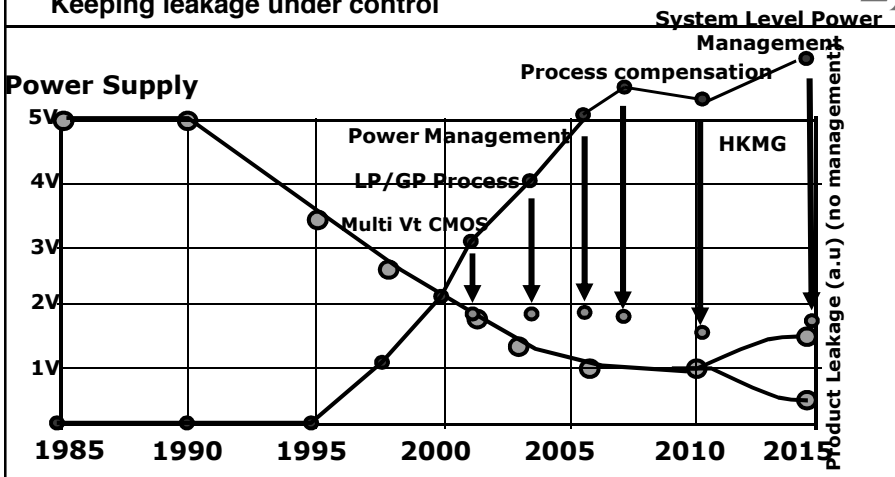
Application / System Solutions
- SW control
- multiple OPP
- Closed loop AVS

Low Voltage / Power Solutions
- Technology: Multi Vt / Large-L / BB
- SRAM: 6T -> 8T/ 0.5V SRAM
- Logic: Low VDD Logic / Async Logic
- IC Design: Design for Variability, GALS, AVS, ABB

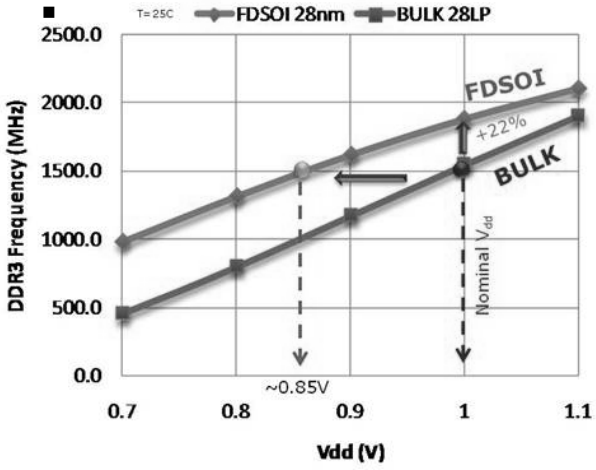
Energy Efficient Design for +/- nominal V_{DD}

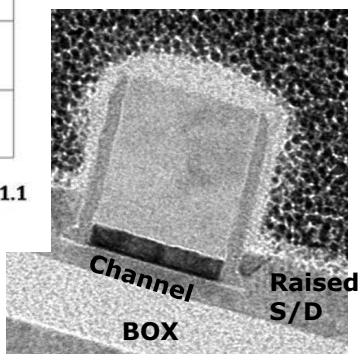
V_{dd} Scaling and energy efficiency

Keeping leakage under control



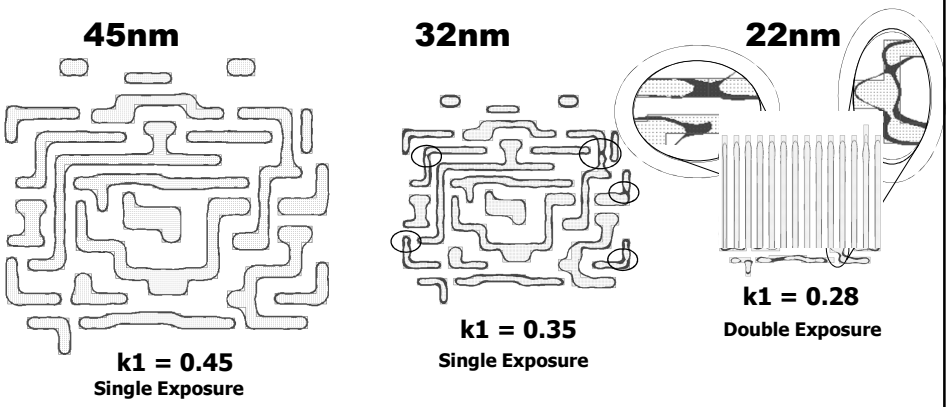
28nm FDSOI: the next speed booster



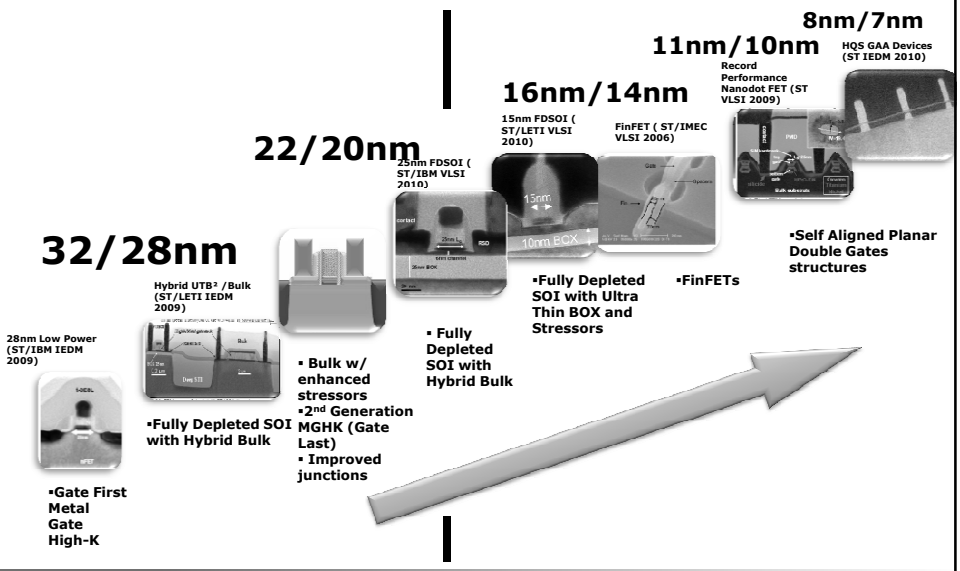


Lithography Scaling

- Reducing k_1 does not come for free!

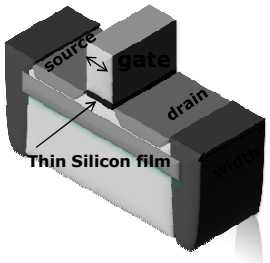


Transistor Architecture Trends

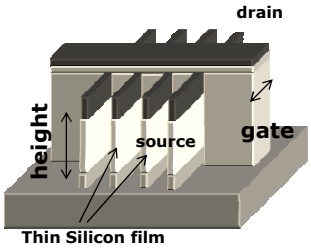


Main candidates after bulk are FinFET and FDSOI:

FDSOI = 2D



FinFET = 3D



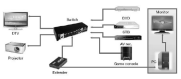
	FDSOI	FinFET
Strengths	- 2D (planar) process - Electrostatic control	-Double gate : Electrostatic control
Risk	- Compatibility with conventional « performance boosters »	-Process complexity (3D) -Compatibility with conventional « performance boosters »

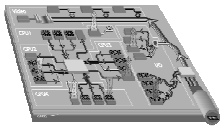
Next to come: 3D, Photonics

- 3D/Heterogeneous Integration of Wide-IO DRAM
- Benefits: Low-Power DRAM/SOC data connexion

Challenges: cost, thermal management, Test, Supply Chain

Photonics on Silicon

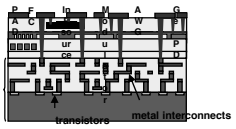




Communication bandwidth rapidly increasing from few Gb/s to 100Gb/s

Optical connexions already present in servers/routers rack to rack

- Copper wire technology not able to sustain such data rates
- Photonics on silicon technology allows die to die and within die optical communication



ST Technology Leadership

- **ST R&D cooperative model allows leveraged capture of technology innovation and risk mitigation**
- **ST leadership in technology enables differentiated / competitive product positioning through:**
  - **Device Integration**
  - **Device add-on for Derivatives / Analog**
  - **Design Enablement**
  - **Specific process modules for best device performance**
  - **Fast yield learning cycle time techniques**

and a full multi sourcing supply-chain efficiency.

SOC CMOS Application Trends : Summary

- SOC Applications require high-performance energy-efficient Processing Units (CPUs, GPUs, …) :
  - Wireless
  - Consumer
  - Automotive
  - Computer Peripherals
- ST's 32/28nm LP / Design Platform at state-of-the-art
  - Process optimizations, above industry leading ISDA HKMG 32nm
  - Library/IP design
  - CAD Flow/ Sign-off optimization
  - Application-driven
- Partnerships are key to optimize R&D investment
  - ***Process, IP, SOC Design, EDA***