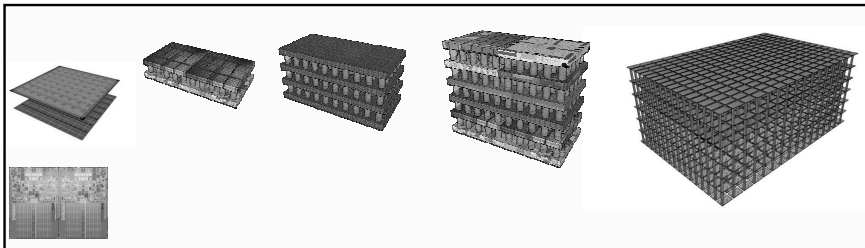
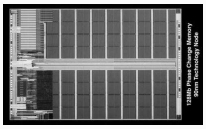
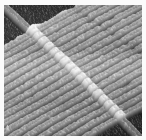
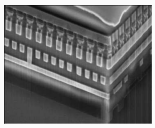


Toward the Design of Robust and Self-Healing Memories



Hsien-Hsin S. Lee
Electrical and Computer Engineering
Georgia Tech





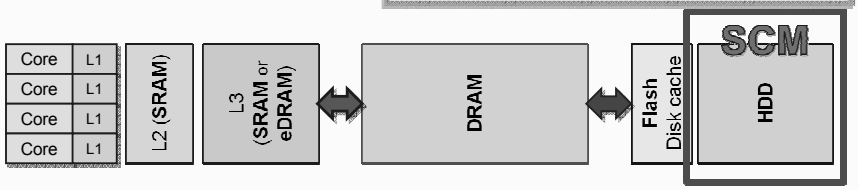
MPSoC 2011
July 4, 2011

Future Memory Trend

- Challenges in scaling conventional DRAM and Flash below 40nm
- New "storage-class memory" is emerging
- Desirable features of SCM
  - Non-volatility (like storage)
  - Solid-state, no mechanical ops (like memory)
  - High density (like storage)
  - High-performance (like memory)
  - Scalable with feature size shrink
  - Low cost (everyone likes money)

So Many Memories, So Many Hierarchy

Memory Type	DRAM	6T SRAM	NOR FLASH	PCM	MRAM	STT-RAM	FeRAM	Memristor
Volatility	Volatile	Volatile	NVM	NVM	NVM	NVM	NVM	NVM
Cell Size (F^2)	6 - 12	50 -80	7 - 11	5 - 8	16-40	6-20	15	scalable
Read	Destructive	Partial Destructive	Non-Destructive	Non-Destructive	Non-Destructive	Non-Destructive	Destructive	Non-Destructive
Erase Granularity	Direct	Direct	Block	Direct	Direct	Direct	Direct	Direct
Write/Erase/Read Time	50ns/50ns/50ns	8ns/8ns/8ns	1µs/1-100ms/60n	10ns/50ns/20ns	30ns/30ns/30ns	20ns/20ns/20ns	80ns/80ns/43ns	1-10us/100us
Programming Energy	Medium	Medium	High	Medium	Medium	Low	Medium	Low?
Write/Read Endurance	~∞/~∞	~∞/~∞	10^6/~∞	10^8~10^{12}/~∞	10^{12}/10^{12}	10^{15}/10^{15} (?)	10^{12}/10^{12}	10^7/?
Multi-Level Cell	No	No	Yes	Yes	stacking	stacking	No	stacking
Cost per bit	Low	High	Medium	Low	??	??	High	??
Supply Voltage	3V	<1V	6-8V	1.5-3V	3V	1.8V	1.9V	<1.5V?

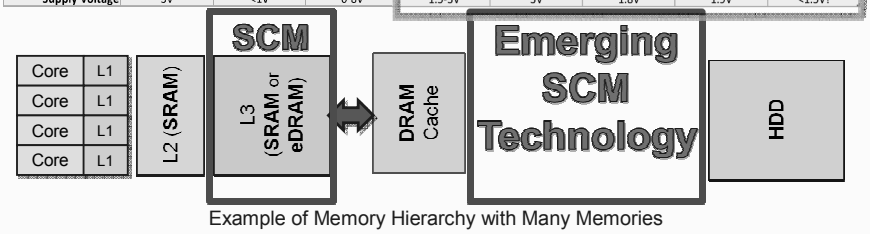


Example of Memory Hierarchy with Many Memories

- Co-optimize: density, speed, reliability, and read/write power
- Some memories can co-locate at the same level
- Probably no one-size-fits-all

Moving SCM Up in Memory Hierarchy

Memory Type	DRAM	6T SRAM	NOR FLASH	PCM	MRAM	STT-RAM	FeRAM	Memristor
Volatility	Volatile	Volatile	NVM	NVM	NVM	NVM	NVM	NVM
Cell Size (F^2)	6 - 12	50 -80	7 - 11	5 - 8	16-40	6-20	15	scalable
Read	Destructive	Partial Destructive	Non-Destructive	Non-Destructive	Non-Destructive	Non-Destructive	Destructive	Non-Destructive
Erase Granularity	Direct	Direct	Block	Direct	Direct	Direct	Direct	Direct
Write/Erase/Read Time	50ns/50ns/50ns	8ns/8ns/8ns	1µs/1-100ms/60n	10ns/50ns/20ns	30ns/30ns/30ns	20ns/20ns/20ns	80ns/80ns/43ns	1-10us/100us
Programming Energy	Medium	Medium	High	Medium	Medium	Low	Medium	Low?
Write/Read Endurance	~∞/~∞	~∞/~∞	10^6/~∞	10^8~10^{12}/~∞	10^{12}/10^{12}	10^{15}/10^{15} (?)	10^{12}/10^{12}	10^7/?
Multi-Level Cell	No	No	Yes	Yes	stacking	stacking	No	stacking
Cost per bit	Low	High	Medium	Low	??	??	High	??
Supply Voltage	3V	<1V	6-8V	1.5-3V	3V	1.8V	1.9V	<1.5V?



Example of Memory Hierarchy with Many Memories

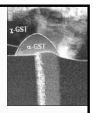
- Co-optimize: density, speed, reliability, and read/write power
- Some memories can co-locate at the same level
- Probably no one-size-fits-all

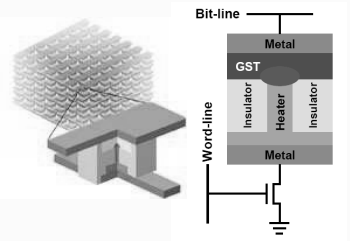
Take

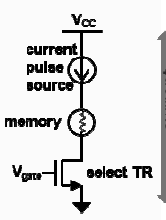
Phase-Change Memory

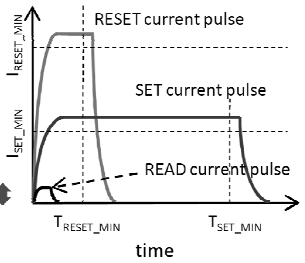
as an example in this talk

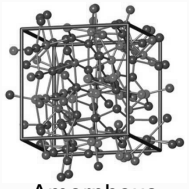
Phase Change Memory (PCM)





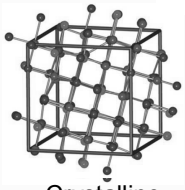






SET

RESET



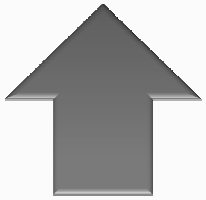
Amorphous
High resistivity
('logic H')

Crystalline
Low resistivity
('logic L')

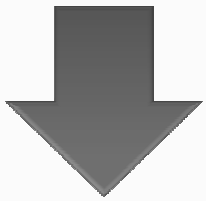
- Chalcogenide alloy (Ge Sb Te)
- RESET >600℃
- SET ~300℃
  (below melting point but higher crystalline point)

Source: Hegedüs & Elliott, Nature Materials & S. Cho in MICRO-42

PCM in Main Memory Hierarchy



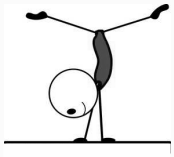
Non-volatile
Bit-alterable
High density (with Multi-Level Cells)
CMOS-compatible process
Better scalability (than DRAM)



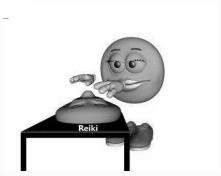
Long read/write latency
MLC read needs serial sensing
MLC write needs iterative writes
Limited write endurance

Enhance Reliability due to Limited Endurance

- **Wear Leveling**
  - Evenly distribute writes
  - Transparent to all components



- **Self-Healing**
  - Dealing with aging stuck-at-faults
  - Continue to use memory with cells stuck-at-value
  - Smart Error Recovery Mechanism



- **Hybrid Hetero-Memory Architecture**
  - Filter out memory accesses
  - Integrate with durability-proof memory (*e.g.,* SRAM)

I. Wear Leveling

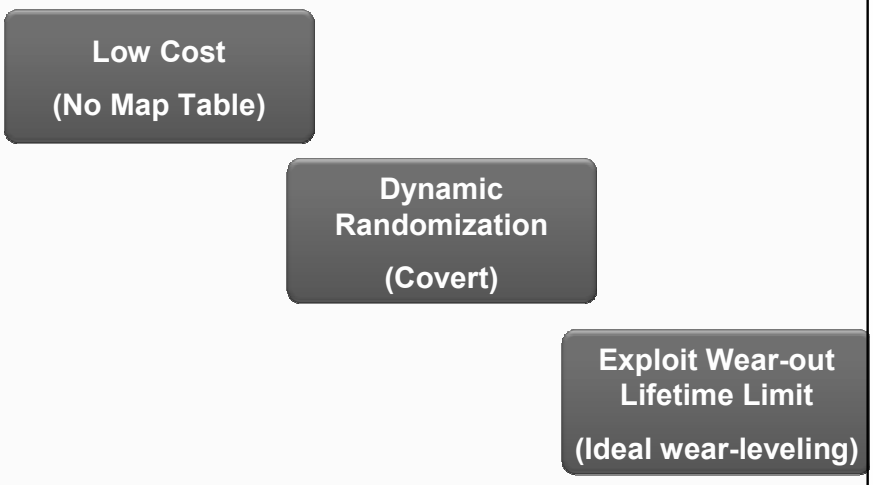
Consider

the *worst-case* scenario

or

a *malicious* process

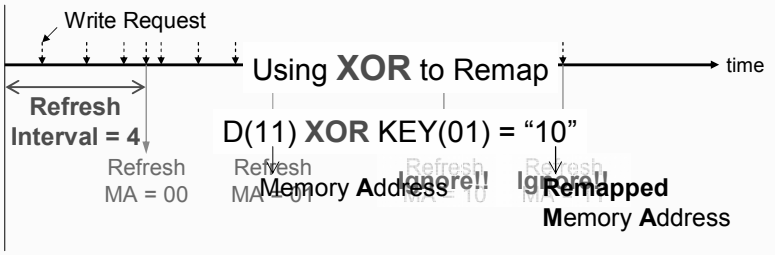
Wear Leveling Design Goals



Security Refresh:
Dynamic Address Randomization

International Symposium on Computer Architecture (ISCA-37)
IEEE MICRO Top Picks 2011

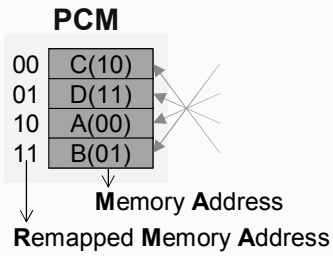
Security Refresh



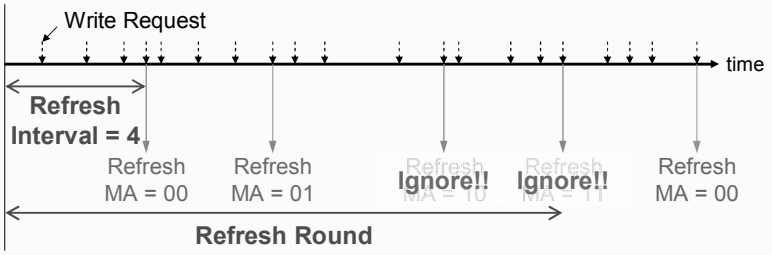
(**P**revious) KEY0 = 01

(**C**urrent) KEY1 = 10

Remap Function: *MA* **XOR** *KEY*



Security Refresh



(**P**revious) KEY0 = 01

(**C**urrent) KEY1 = 11

Remap Function: *MA* **XOR** *KEY*

PCM

00	C(10)
01	D(11)
10	B(01)
11	A(00)

Memory **A**ddress

Remapped **M**emory **A**ddress

Security Refresh

Dynamic Remapping

Remapped by Key = 01

00	B(01)
01	A(00)
10	D(11)
11	C(10)

Remapped by Key = 10

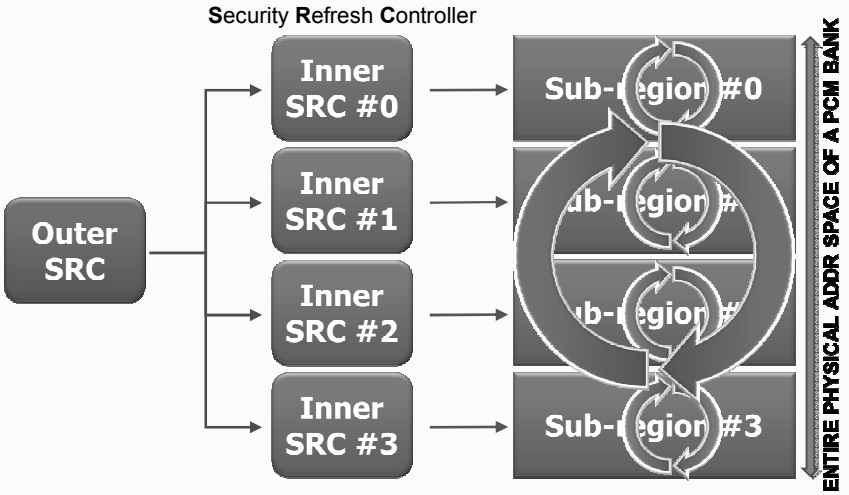
00	C(10)
01	D(11)
10	A(00)
11	B(01)

Remapped by Key = 11

00	D(11)
01	C(10)
10	B(01)
11	A(00)

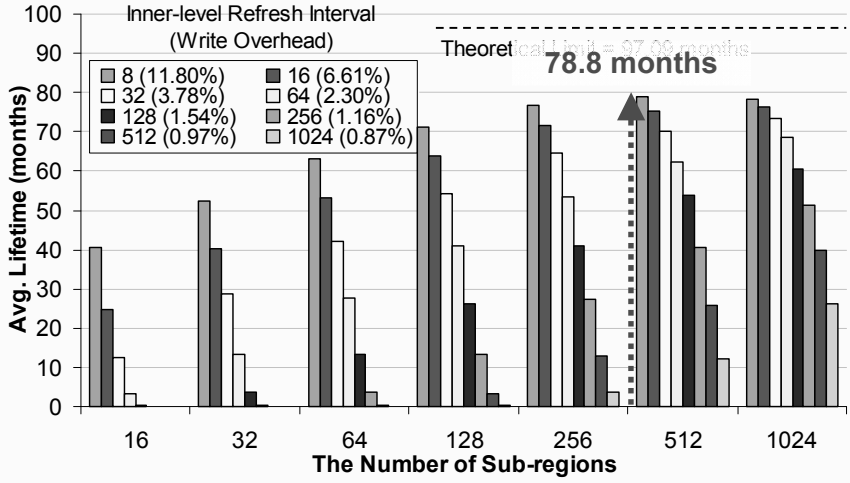
Security Refresh Round (*i*) | Security Refresh Round (*i*+1)

Two-Level Security Refresh



15

Two-Level Security Refresh Evaluation



16

II. Self-Healing

Continue to operate the memory even when cells are *stuck-at-value*

SAFER:
Stuck-At-Fault Error Recovery

International Symposium on Microarchitecture (MICRO-43)

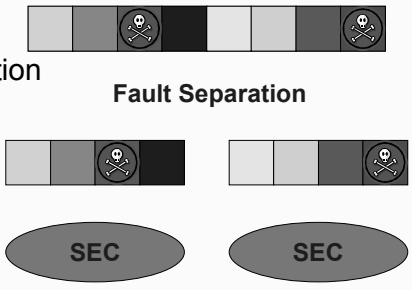
SAFER:

1. Fault Separation

2. Single Error Correction

Basic Concept of SAFER

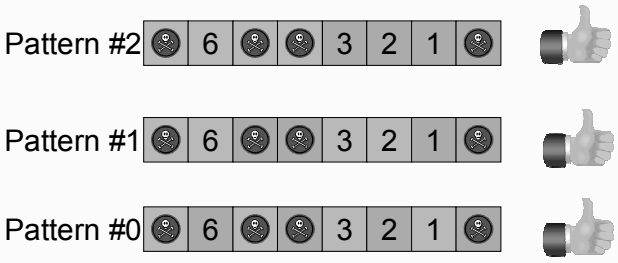
- Multiple error correction
  - Fault separation
  - Apply Single Error Correction (SEC)



- Exploit properties of Stuck-At Faults
  - Permanency
  - Readability

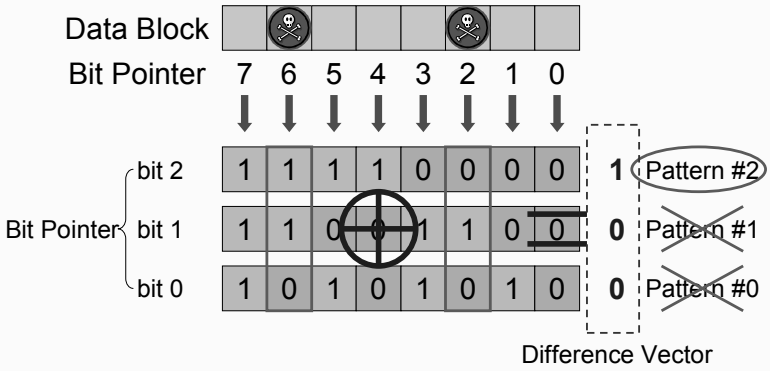
Fault Separation

- Assuming 2 faults in an 8-bit block
  - C(8,2) = 28 possible fault pairs
- How to separate these 2 faults (of all 28 pairs)?



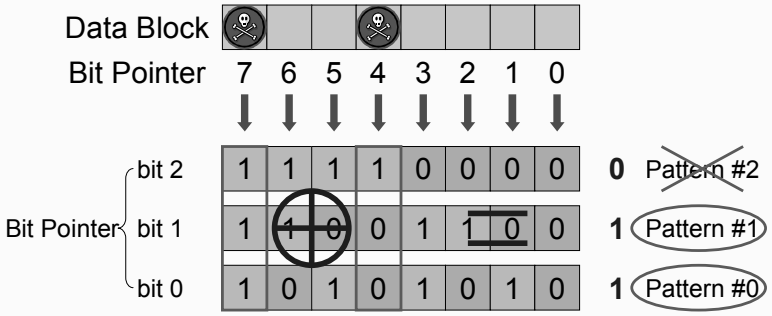
Decision for Fault Separation

- Find pattern candidates by **XORing** bit pointers



Decision for Fault Separation

- Find pattern candidates by **XORing** bit pointers

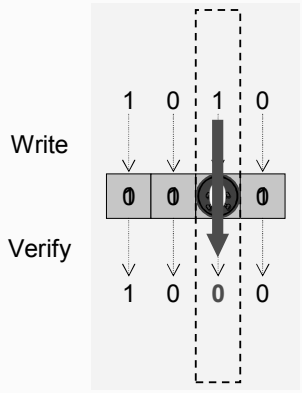


SAFER:

1. **Fault Separation**
2. **Single Error Correction**

Low-cost Single Error Correction

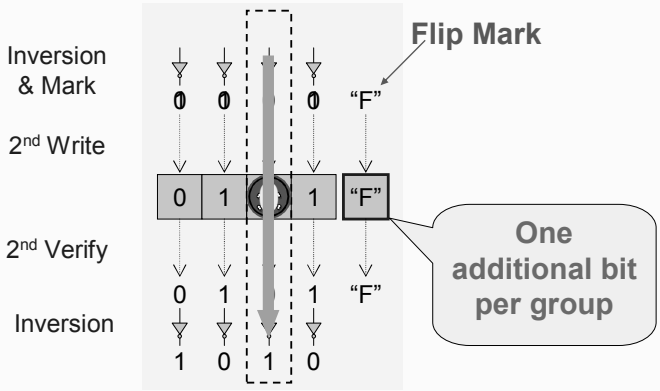
- Stuck-At Fault Property: Readability



Need to recover!!

Low-cost Single Error Correction

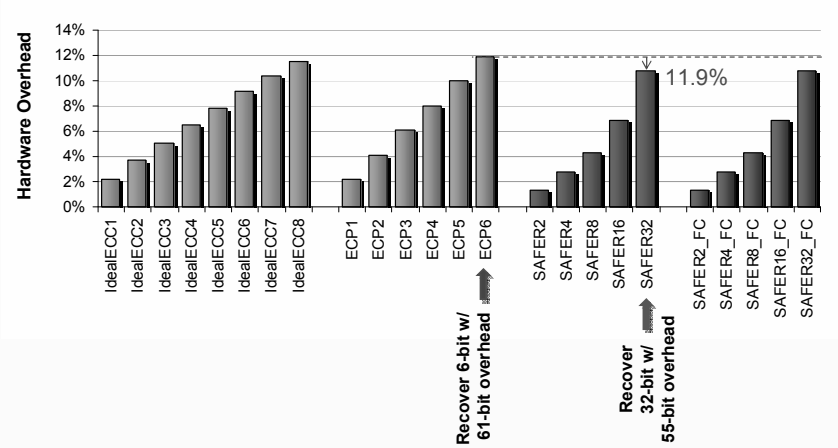
- Data Inversion as an SEC



Recovered from Stuck-At Fault!!

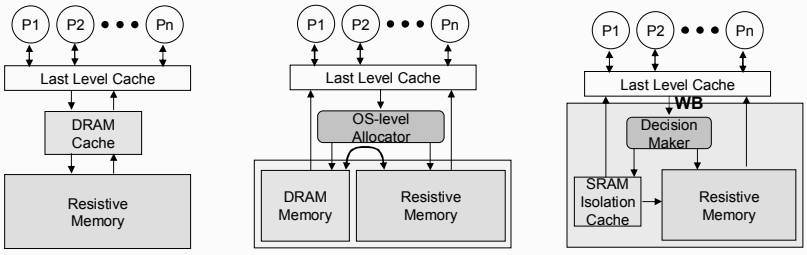
Hardware Overhead vs. Recoverability

- Data block size = 512 bits
- IdealECC, ECP, SAFER, SAFER_FC



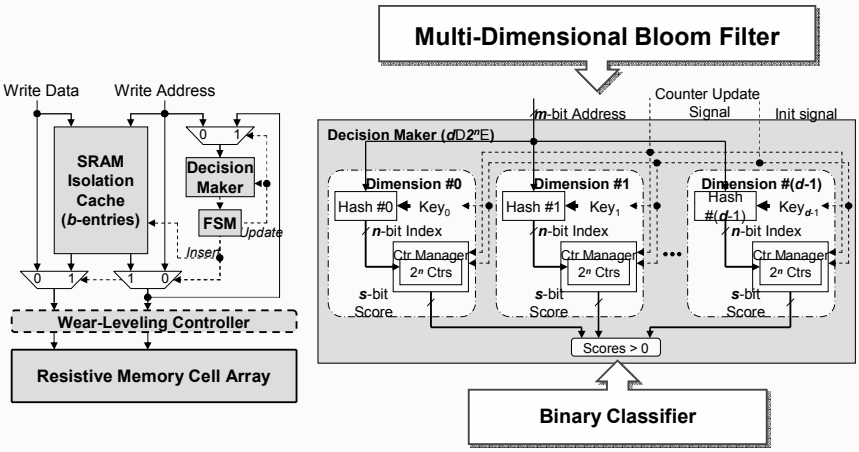
Hybrid Resistive Memory

Hybrid Resistive Memory Architecture



Serial Parallel Selective

Multi-Dimensional Address Classification



SUMMARY

- SCM will have a role in memory hierarchy
- **Design for Reliability** is top priority
- **Enabling Technologies**
  - Security Refresh: Randomized Wear-Leveling
  - SAFER: Dynamic Multi-Error Recovery
  - Hybrid Resistive Memory Architecture

That's All, Folks!

Georgia Tech
ECE MARS Lab
http://arch.ece.gatech.edu