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Session 5: Keynote Speech

Design Technology for Future Computing Systems

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  - **Platform/Integration & Devices: C.C. Wu**
  - **Advanced Transistor Research: Clement Wann**

Outline

- Design Trends for Computing Systems
  - Performance & Power
  - Server/Desktop, Graphics, Mobile
- Design Technology
  - Standard Cells Library
  - SRAMs
- Scaling at System-Level
  - 3D ICs
- Scaling in SoC: Moore's Law continues
  - 3D transistors: FinFETs

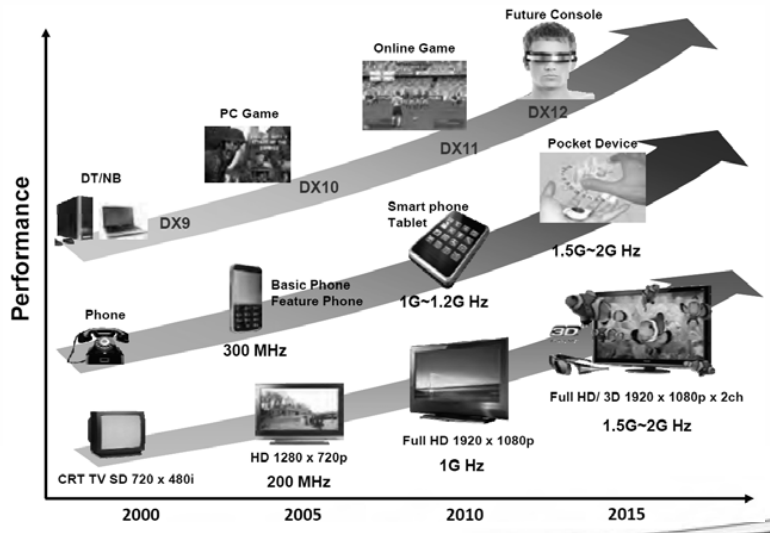
Trend for Future Computing Systems

- Unending demand to integrate more processing, graphics, video and specific function blocks.
- The trend each year is to provide
  - Higher Processor performance levels
  - Higher Memory bandwidth
  - Higher Network bandwidth
  - Lower Computing System Power

Trends for Computing Systems

TSMC Property

- Ever growing integration of more processing, graphics, network Gb/sec, video, audio, crypto, …



Technology Trend for Future Computing Systems

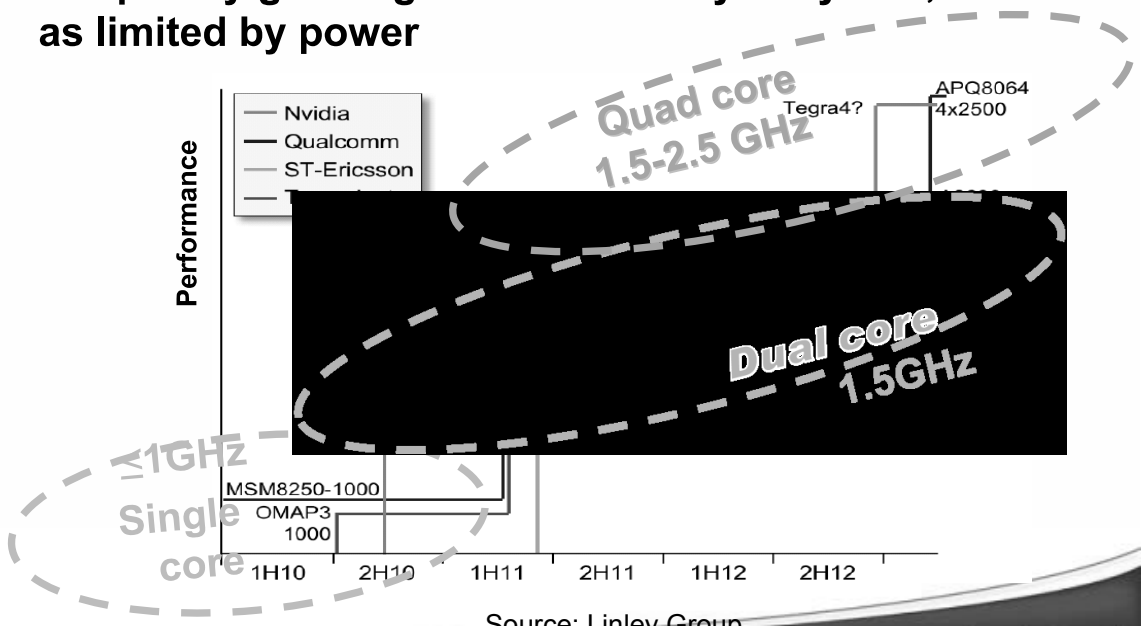
TSMC Property

- Each year provide <u>higher</u>:
  - Processor performance,
  - Graphics and Video realism,
  - Memory bandwidth,
  - Network bandwidth, <u>BUT</u>
- At <u>no higher</u> system:
  - Power
  - Costs

Mobile SoC Performance Trend

TSMC Property

- Processor core count doubling every 2-3 years
- Frequency growing ~500 MHz every 2-3 years, as limited by power

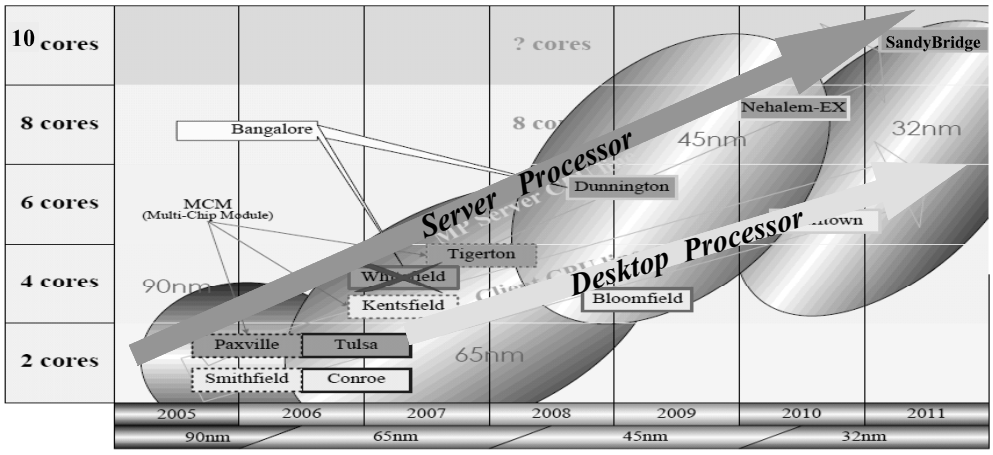


Source: Linley Group

Server and Desktop Processor Trend

TSMC Property

- 2 CPU cores growing to 10^{+} in just 6 years
- Cache size growing from 512KBytes to 32MBytes
- Adding GPU, Video, Connectivity, audio, …

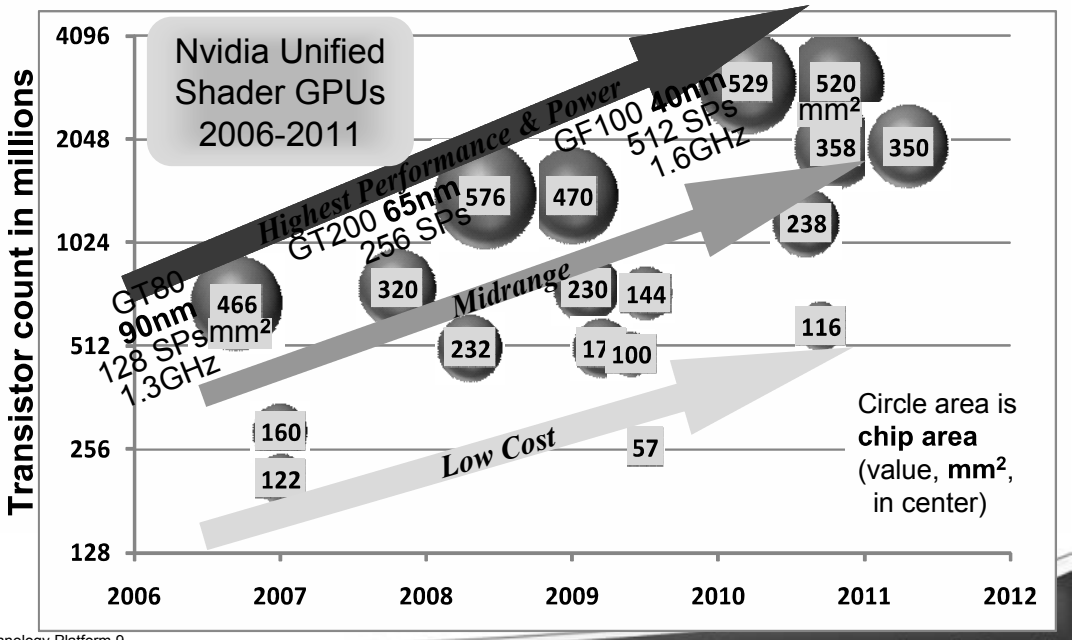


Source: Hiroshige Goto, PC Watch

Graphics Trend

TSMC Property

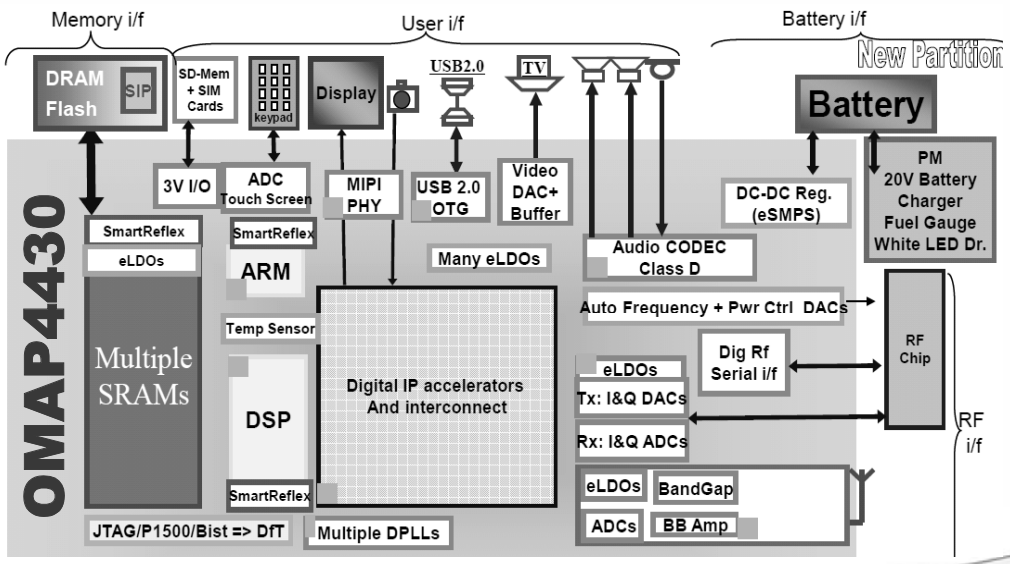
- **More Performance, more Stream Processors**



Mobile SoC Integration Trend

TSMC Property

- **SoC chips integrating: GPU, video, audio, mixed signal, base-band, voltage regulators, …**

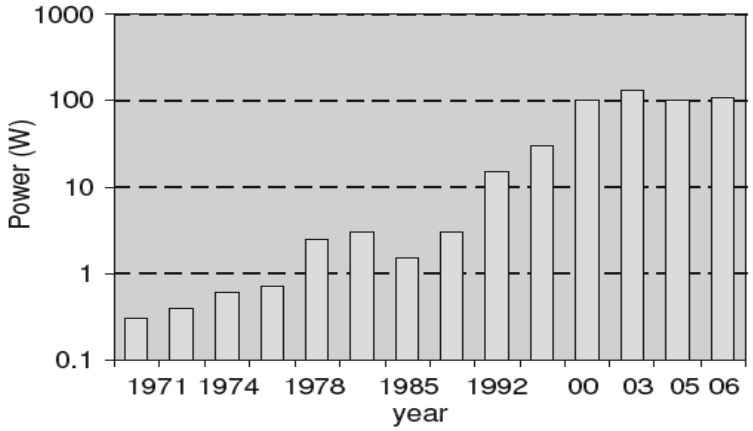


Source: Hot Chips Symposium

Power Dissipation Trend: Products have reached technology's ceiling!

TSMC Property

- **Servers & desktops, even with fans and heat pipe:**



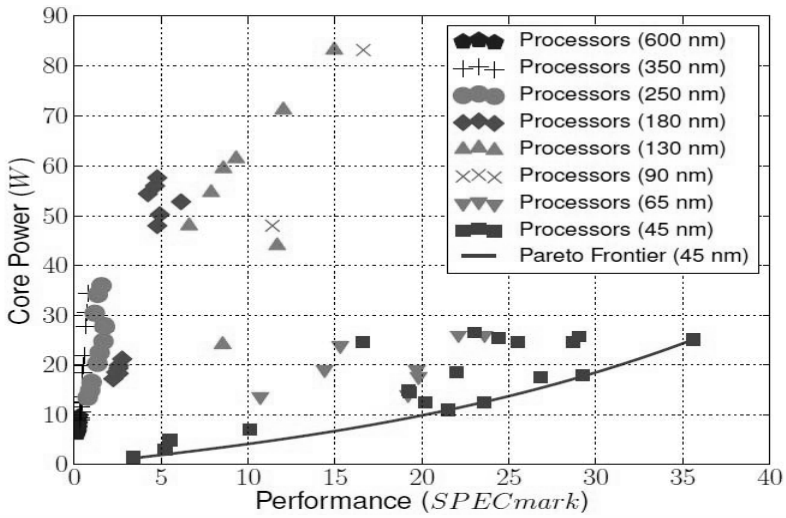
Power consumption of Intel microprocessors from 1970 to 2006

[ASP-DAC 01, ISSCC 03, 04, 05]

- **Mobile ceiling much lower, also battery limitations**

What Happened from 90nm to 65nm?

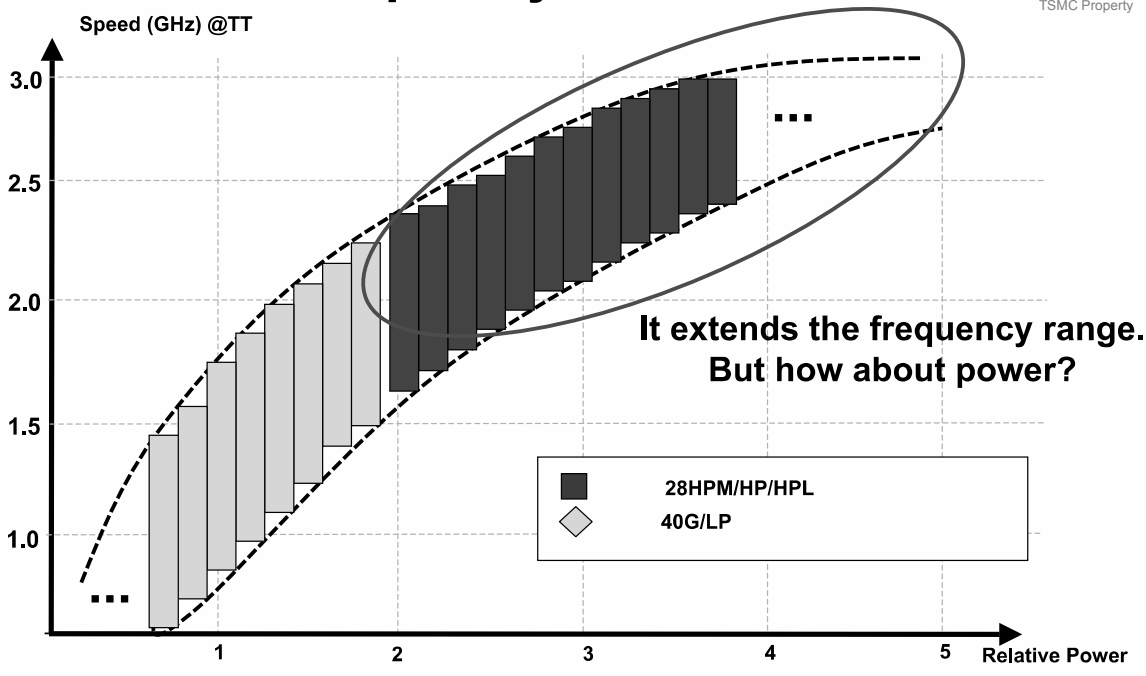
TSMC Property



Intel Processors power and performance per core

Source: "Dark Silicon and the End of Multicore Scaling" by Hadi Esmaeilzadeh, et al, Proceedings of 38th International Symposium on Computer Architecture (ISCA '11)

Cortex A9 Frequency and Power Trend



Innovation Trends

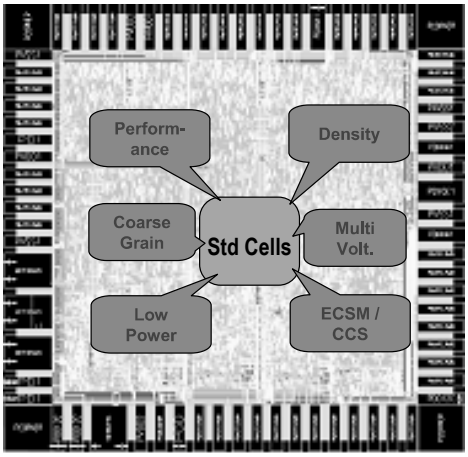
- Innovations from Foundry (e.g. TSMC)
  - SSTA, High-K metal gate, …..
  - More-than-Moore, 3DICs
- Innovations from Design/Systems Industry
  - Clock gating, Power gating
  - Parallel computing
    - Multi core, heterogeneous system
  - System level power management
  - Software/OS power management
  - … and more …

Summary on Design Methodology

- Future computing systems require the integration of more functions onto semiconductor chip(s)
- The need for more transistors on a chip easily meets the growth of 2x transistors every 2 years
- Power is limiting Computing System growth
- TSMC with industry innovators must push Moore's law together
  - Into 14 nm node, 11nm node, and beyond
  - From 12-inch to 18-inch wafers
- Offering better computing power with lower cost at regular intervals is what keeps Future Computing System growth exciting

Standard Cell Libraries

- Optimized to technology
- Early available & continuous improvement
- Include high performance, high density and low power cells and solutions
- Multi-VT, Multi-VDD, Multi-Track solutions
- DFM compliant
- Support major EDA tools
- Layout-effect considered for characterization
- Compact size in industry



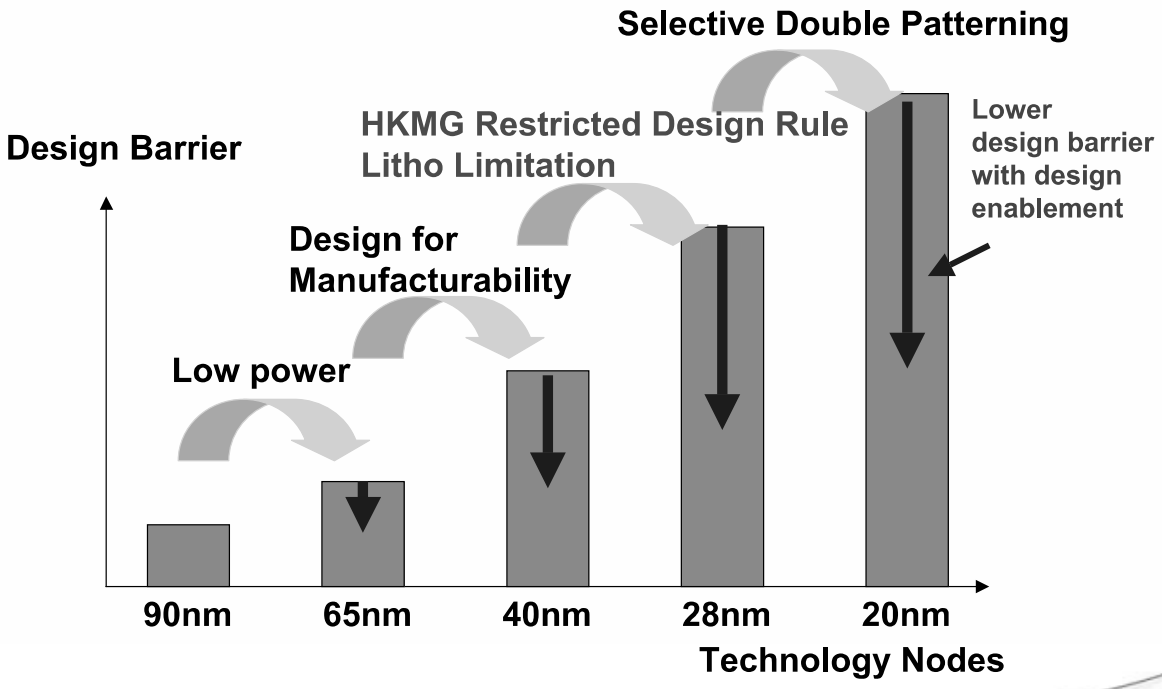
Special features in Std Cells for advanced nodes

TSMC Property

- Further Restricted Design Rules (RDR)
  - Fixed Poly Pitch/Space
    - Use poly pitch in x-direction
  - Poly jog is not allowed
    - Use M2 in vertical direction as intra-cell connection
  - Uni-direction poly: no horizontal poly for routing
    - Cannot use poly for intra-cell connection

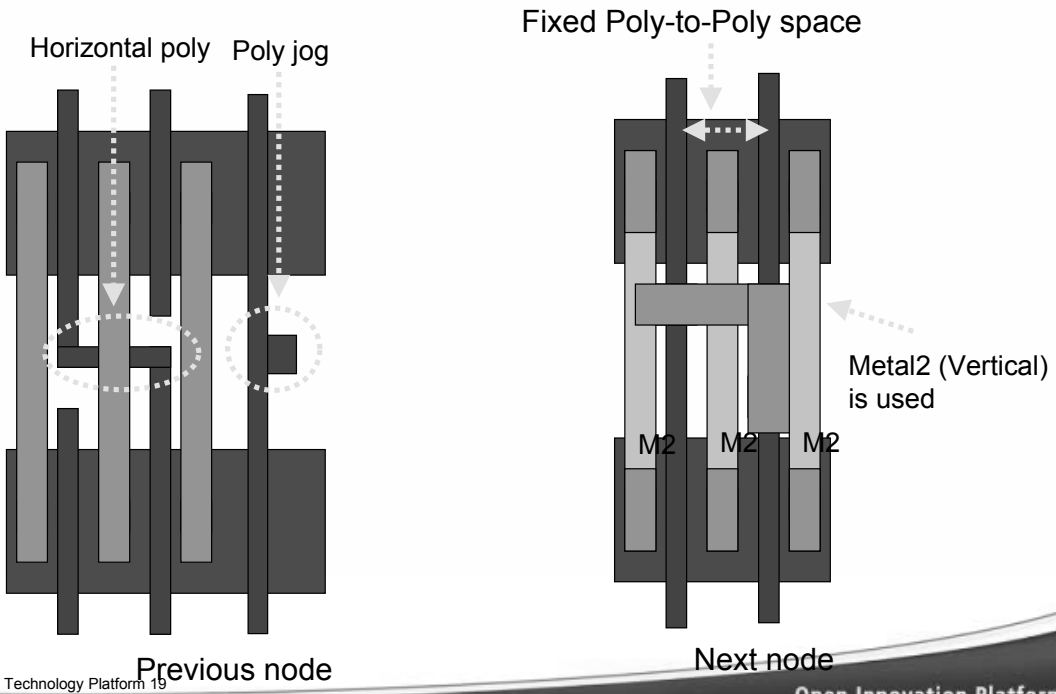
Illustration on Design Challenges

TSMC Property



Node-to-node Layout Comparison

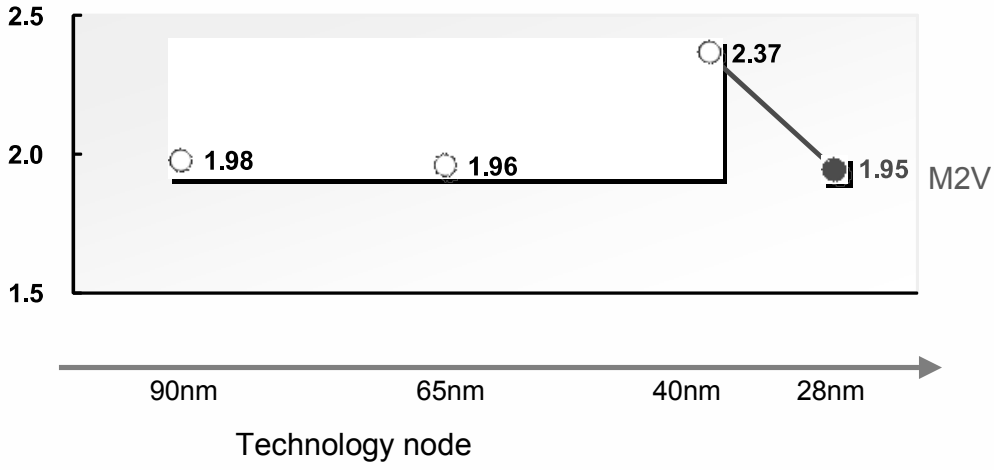
TSMC Property



Gate Density Shrink Ratio

TSMC Property

- **M2 is utilized for mitigating 28nm RDR limitation**



* Raw Gate Density: 40% SDFQD1 + 60% ND2D1

Std Cell Library Features

Gate Bias

LVT

HVT

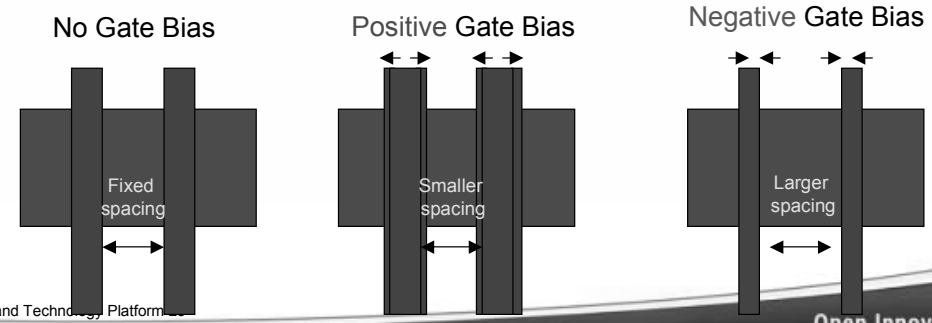
SVT Multi-VDD Library		Coarse-Grain Library
Base Cells	Multi-VDD Cells	Coarse-Grain Cells
Buffers Boolean Combinational Arithmetic Sequential Filler/De-cap ECO Antenna Diode	Up Level Shifter Down Level Shifter Isolation Cell	Header Footer Always-On Cells Retention Register

Low Power Solution

Design Strategies	Advantage	Special Cells Required
Multi-Vt	Lower leakage	Multi-Vt libraries
Voltage Scaling	Less Dynamic Power	Level Shifter Isolation Cell
Power Gating	Lower leakage	Power Switch Retention FF AON Cell

Gate Bias – New Solution of Speed & Leakage

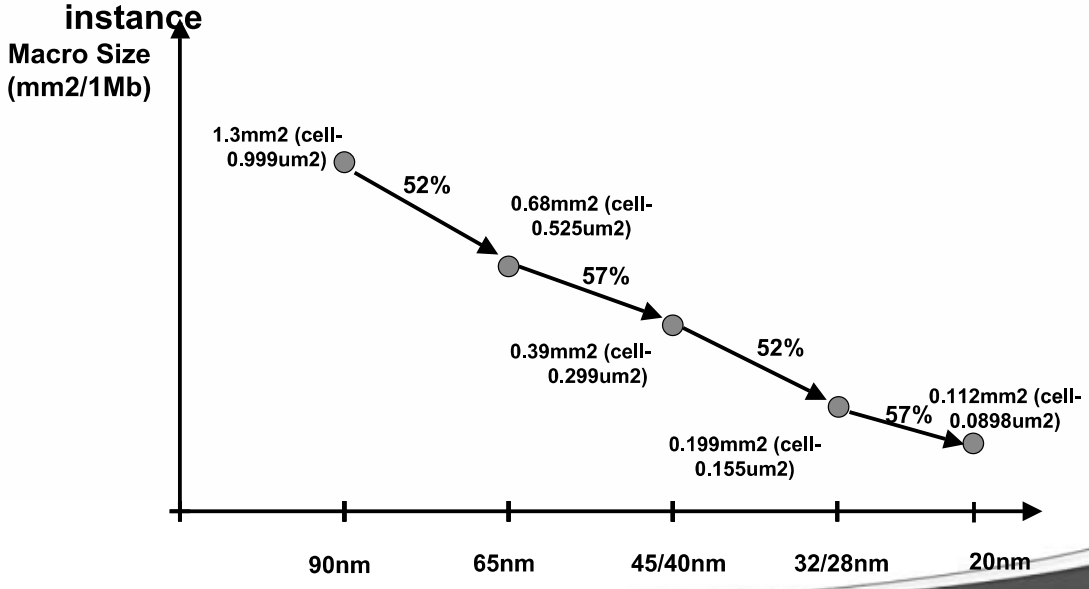
- **Positive and negative gate bias solutions are provided in N28 library.**
  - **Positive gate bias – Increase gate length. Speed ↓ , Leakage ↓**
  - **Negative gate bias – Reduce gate length. Speed ↑ , Leakage ↑**
  - **Gate bias library is footprint compatible with other Vts, only add one extra layer in GDS and no extra mask is required.**
- **Gate bias solution provides more flexibilities for designers – using single Vt + gate bias to achieve speed and leakage requirement.**



SRAM design challenges at advance nodes

Macro Area Shrink Ratio – 90nm to 20nm

- **(one cell-size flavor example) Maintain 80% cell efficiency, bit cell size shrink ratio determines the macro shrink ratio in 1Mb instance**



SRAM Design Issues and Solutions

Issues	Solutions
Local variability with increasing density	Statistical simulation with 5-6 σ coverage
RDR causing array efficiency degradation	Fully utilize poly cut. Double cell pitches as one layout unit in a mux1-2 design
Increasing leakage/active current in macro level	35nm Lg in word-line drivers for speed/leakage optimization
Vmin support for DVFS application	0.24um2 2P mux1 cell for Vmin down to 0.8*V_nom, or dual rails with 0.127um2 cell
Speed degradation at WCL	0.24um2 2P mux1 cell for high speed

(New) SRAM Design Issues & Solutions

Issues	Solutions
High poly resistance	Use short poly fingers. No poly or M0 routing for critical blocks.
High metal resistance	Segment WL or WL repeaters for large macros.
Vccmin support for DVFS applications	Read/write assist circuitry or 2P mux1 bit cell.
Increasing variability	Statistical simulations for 5-6 σ coverage. AC write Vccmin simulations to ensure proper WL pulse width.
G-rule compliance for WL driver	Jump to different metal layers.

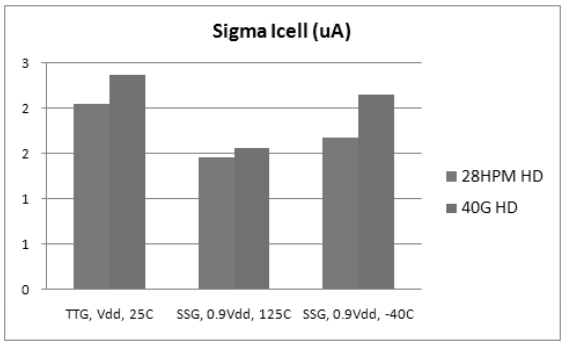
SRAM Low Vccmin consideration

- **Larger bit cell (6T)**
  - **0.145μm²**
- **2P mux-1 bit cell (8T)**
- **Custom bit cell/sequential elements following logic rule for small arrays (e.g. < 1Kbits)**
  - **8T, 9T, 10T**
- **Assist circuitry to improve Vccmin**
  - **Bit cell optimized for read Vccmin before applying Design Assistance**

High Sigma Design

TSMC Property

- Thanks to HKMG, σ (Icell) improved but memory density doubles, 6 σ design margin should be considered for 16Mb SRAM array
- Defining sigma coverage (sigma number, Z) based on bit density and yield requirement
- Including of worst bit condition in characterization and verification for design robustness



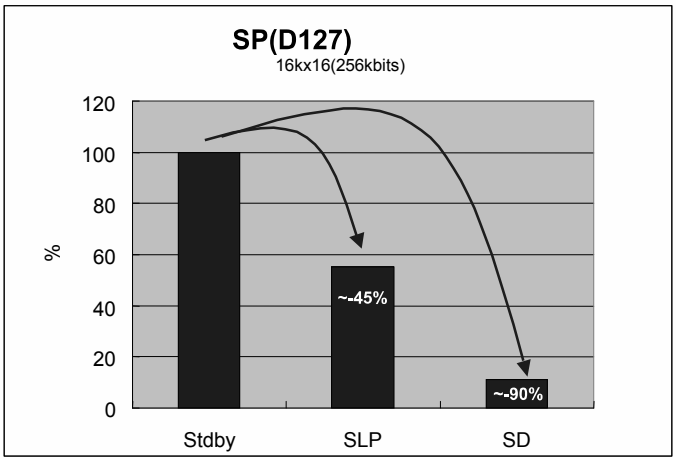
Read/Write Assist Circuitry

TSMC Property

- on ARM test chip
  - Data-aware write assist & body bias for bit cell nwell
  - Mainly to enable post silicon Vccmin modeling learning
- on advanced Process Qualification test chip
  - Write assist
    - Lower CVDD
    - Negative BL
  - Read assist
    - Bit tracking WL underdrive
- Schemes investigated (on-going)
  - Bit cell body bias control (significant area penalty)
  - BL pre-charge level (does not yield Vccmin improvement as claimed)
  - Boost CVDD (significant power penalty at high temperature)

Low Leakage Solutions

- 35nm Lg in word-line drivers to optimize active/leakage power
- Sleep mode to shut down periphery circuits
- Shut-down mode to totally cut off the current path to array and periphery

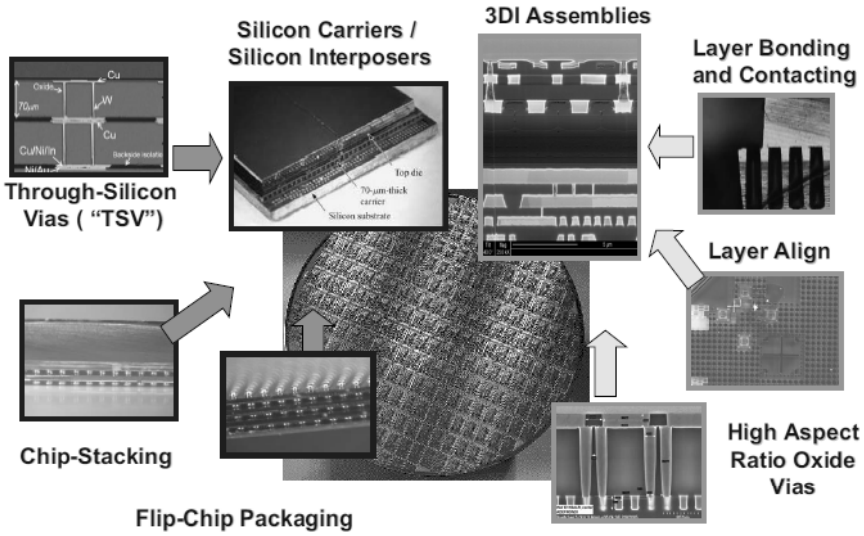


(Advance node) Low Leakage Solutions

- **Continue to support existing solutions including long Le WL driver, sleep mode for peripherals and shutdown mode for entire arrays**
- **Explore deep sleep mode to lower CVDD for bit cells while retaining states**
  - **Additional 15% saving on top of sleep mode**
- **Implement fine grain sleep mode in large macros**
  - **Unused segments stay in sleep mode**

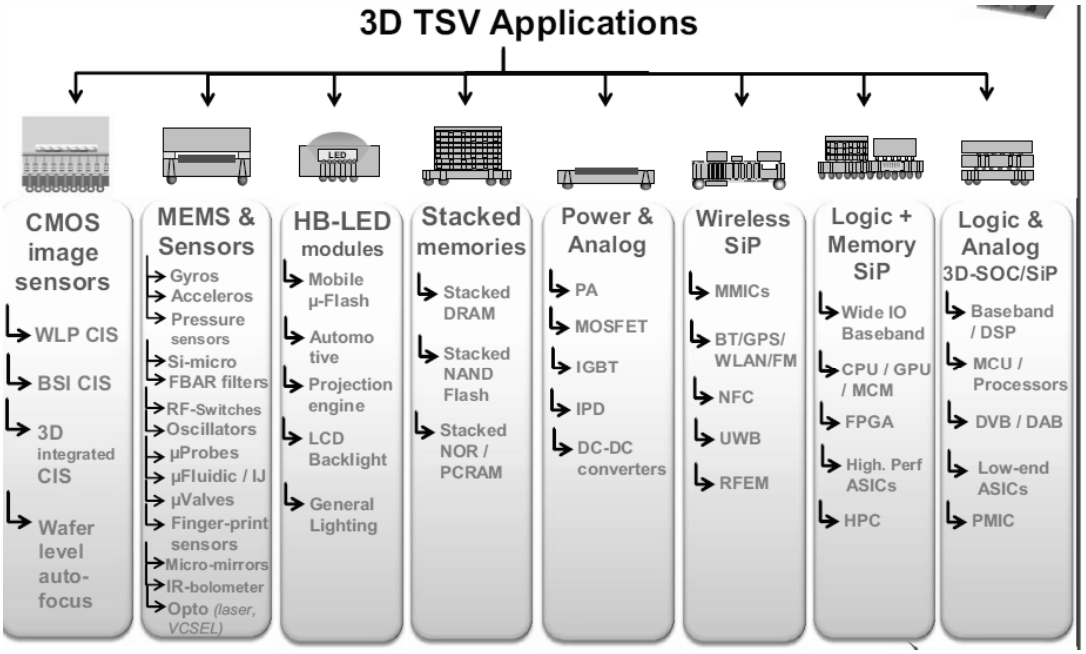
On 3D ICs

Technologies for 3D Integration



Source: Jeff Burns, "3D Integration- A Server Perspective," IEEE 3DIC Conference, 2010

Application for 3D Integration



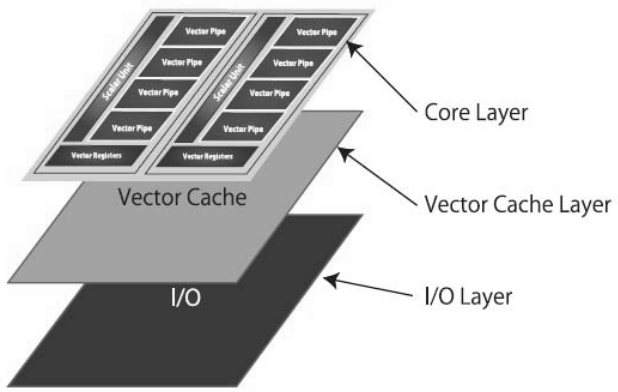
Source: Christophe Zinck, "3D Integration Infrastructure & Market Status," IEEE 3DIC Conference, 2010"

3D System Development Approach

- **Development and Optimization of 3D Systems requires a Cross-Disciplinary Approach**
- **3D system architecture**
  - **System partitioning across chips**
  - **Leverage Capacity, Bandwidth, Latency**
  - **Power/Thermal Considerations**
- **3D chip design**
  - **Design Ground rules & Methodology**
  - **Power Delivery, Clocking, I/O, Design IP**
  - **Design Tools**
- **3D technology development**
  - **Through Silicon Via, Wafer finishing,**
  - **Micro/Mini-C4, Bond & Assembly**

Multi-Processor

- **Eight-cores MPs are already in the commercial market, and an eighty-cores CMP is prototyped by Intel .**



3D IC Topics-Design & System

direction	topics	items
3D IC system	architecture	processor and memory integration, memory stacking,, vector processor, muti-cores
	application	Image sensor, signal processing
Design and verification flow	flow	multiple model integration 3D logic-to-logic placement
	Power	Power distribution network design, analysis IR-drop and Xtalk evaluation and suppression
	Timing	Performance analysis and optimization for 3D multiple cores uPs
	Thermal	Thermal Management of 3D Multi-core System
	Design kits for 3D IC	3D DRC/LVS
	Cost	Cost effectiveness of 3D integration options

3D IC Topics: Process, Test and Bonding

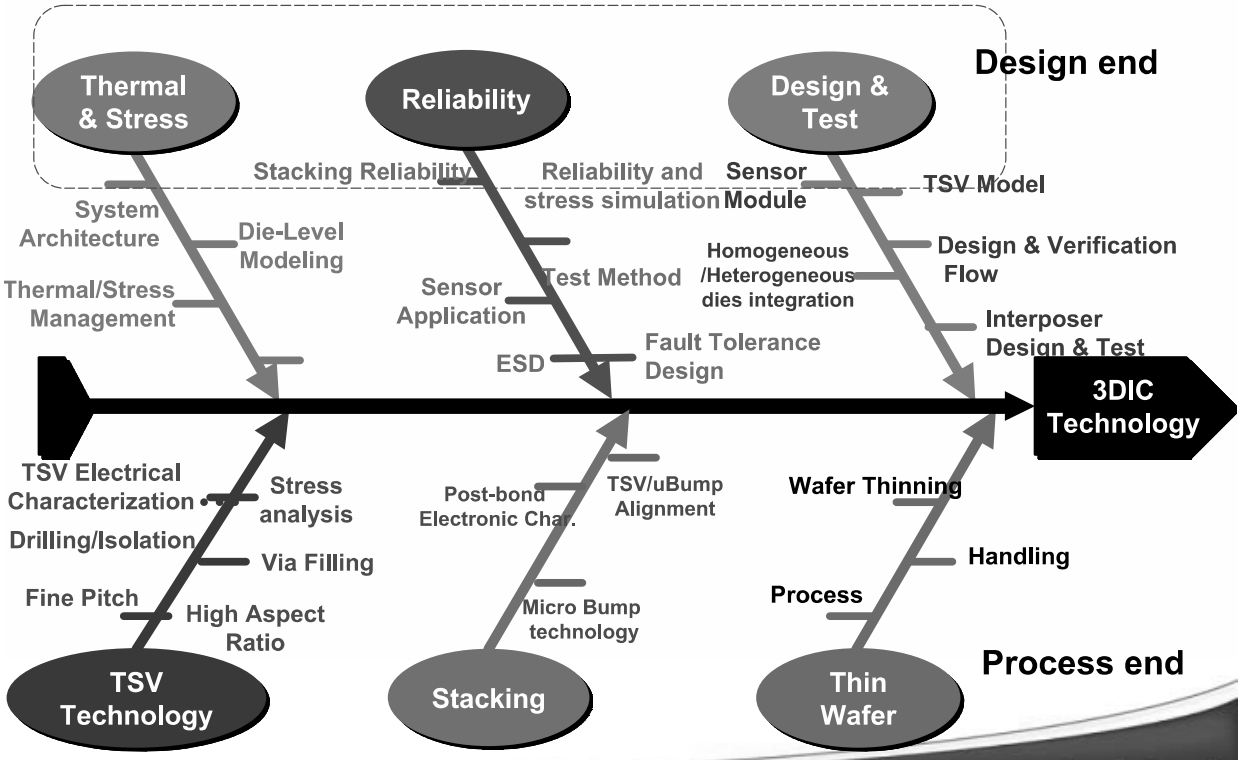
direction	topics	items
Process	**Interconnection**	**Etching and fill process for high performance 3D interconnection**
	TSV process	**Low-capacitance TSV, low-cost**
	Silicon interposer fabrication	**TSV-based si-interposer, high-density Cu-filled TSV**
	Bonding and uBump	**Alignment** **Stress induced by uBump**
Test	**DfT and measurement**	**3D DfT architecture** **Test sequence for TSV** **Pre Bonding metrology solution and using optical metrology** **Contactless:** Transceiver for Wireless Testing Systems
	Others	**Wireless power transfer**

3D Integration Design Implications

- **Chip infrastructure elements:**
  - **Clock distribution, power and ground distribution**
- **IP blocks:**
  - **SRAM, eDRAM, and non-traditional array technologies**
- **Custom and random logic**
  - **Within-stack and on- and off-socket bussing and I/O**
  - **Analog, special-purpose functions, materials**
- **Design know-how, and supporting methods and tools:**
  - **Early and detailed planning and partitioning**
  - **Electrical and physical optimization and design**
  - **Automation-enhanced implementation**
  - **Checking and verification**
  - **Capture of power & thermal effects**

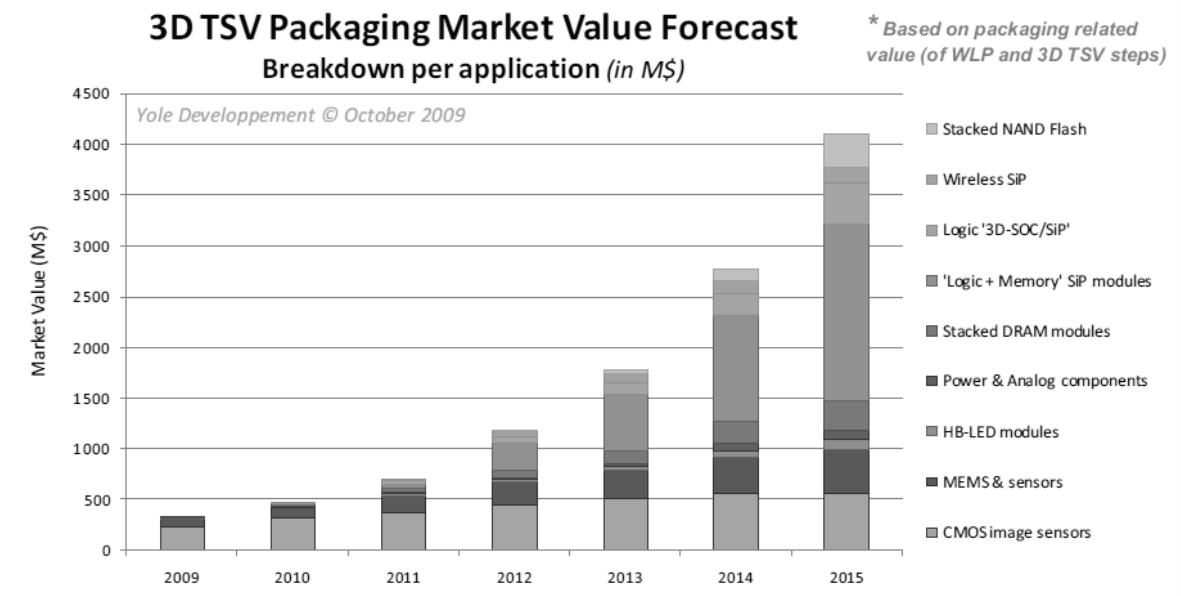
General 3D IC Enabling Technology

TSMC Property



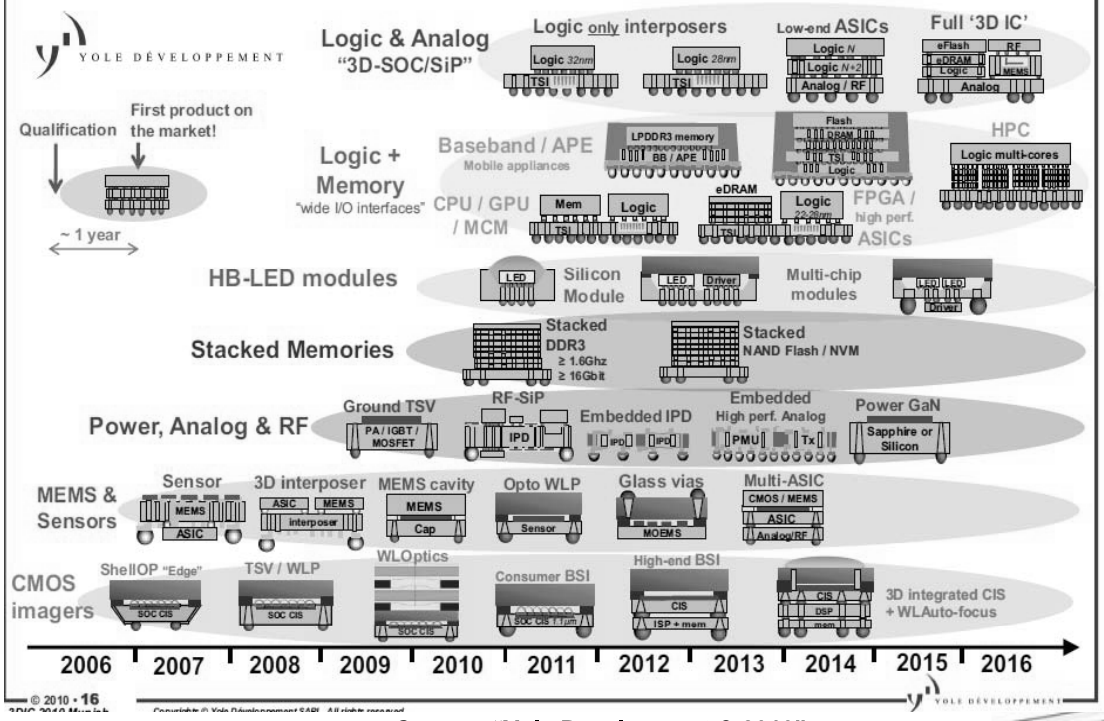
3D TSV Packaging Market Value Forecast

TSMC Property



Source: Yole Development © 2009"

Global Roadmap for 3D Integration with TSV



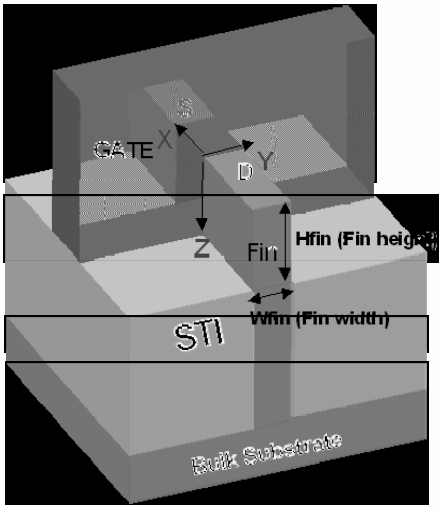
Source: "Yole Development © 2010"

Why FinFET for More Advance Node?

- **Better electrostatics characteristics enable gate length scaling**
- **Intrinsic benefit of better swing and less dopant fluctuation enable low V_{DD} operation**
- **Sidewall channel provides extra current gain in SRAM and narrow width devices.**

FinFET device

TSMC Property



- Bulk FinFET architecture
- (100) substrate
- Standard notch orientation
- Transistor module
- Optimized HK/MG gate stack
- Dual epitaxy
- Gate pitch
- Fin pitch is (spacer pitch halving)
- Wfin, Hfin

Source: 2010 IEDM, C.C.Yeh, et al.

Challenges for FinFET devices

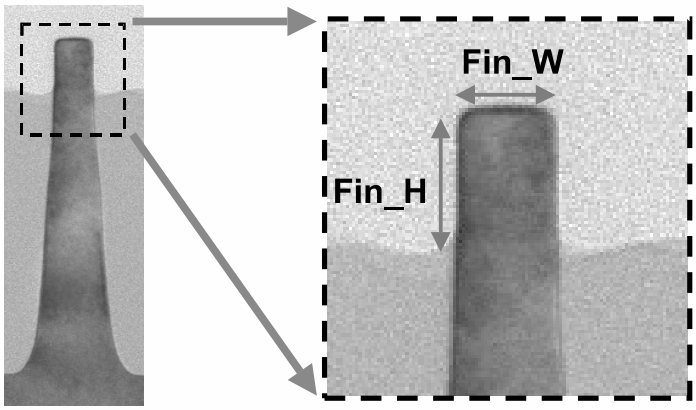
TSMC Property

- Stressor implementation in 3D structure
- Dual workfunction metal implementation in tight-pitch
- Epitaxy S/D quality on different crystalline planes
- Design difficulty caused by digitized fin numbers

Source: 2010 IEDM, C.C.Wu, et al.

Fin Structure Definition

TSMC Property

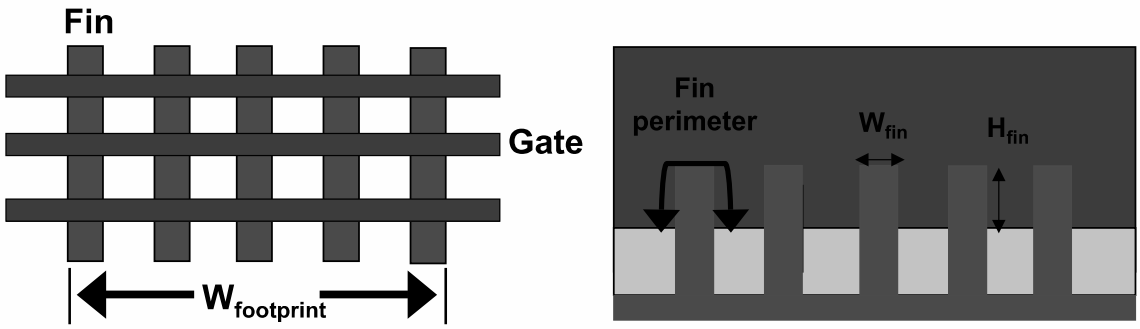


- **Effective width = 2 x Fin_height + Fin_Width**

Source: 2010 IEDM, C.C.Wu, et al.

Denomination of "Widths"

TSMC Property



W_{fin} = physical fin width
W_{eff} = Σ (fin perimeter)= Number of fins x (W_{fin} + $2H_{fin}$)
$W_{footprint}$ = real Si estate

- **FinFET has potential to gain drive current by larger effective width over planar on the same layout footprint.**

Source: 2009 IEDM,C.Y. Chang, et al.

Summary on FinFETs (2010 IEDM paper)

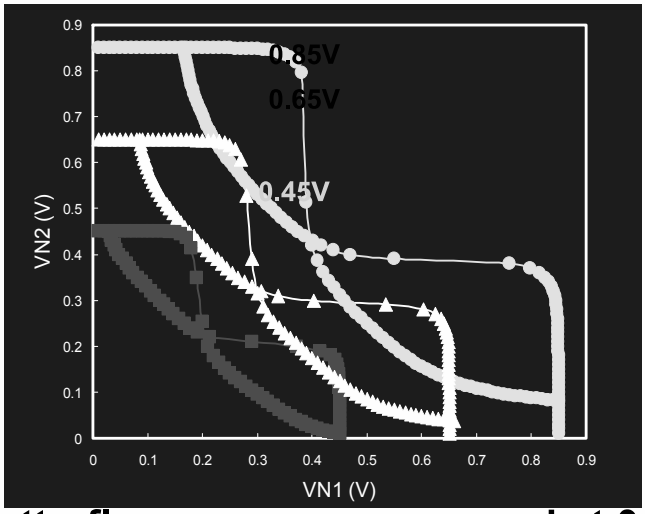
TSMC Property

- Dual-Epi raised S/D
  - low R_{sd} for both N/P
  - SiGe strain engineering for P
- Dual-WF HK/MG stack
  - Good electrostatic control down to 20nm L_{gate}
  - Replacement-gate further boosts PFET performance
- Balanced and competitive N/P I_{on}-I_{off} performance
  - N / P I_{on} achieve 1200 / 1100 μA/μm @ I_{off} = 100nA/μm @1V
- Excellent SRAM SNM at 0.45V V_{dd}
- Challenge: process in 3D structure and design difficulty caused by digitized fin numbers

Source: 2010 IEDM, C.C.Wu, et al.

SRAM Butterfly Curve

TSMC Property



Source: 2010 IEDM, C.C.Wu, et al.

- Butterfly curves are measured at 0.85V, 0.65V and 0.45V respectively
- Cell is functional down to 0.45V V_{dd} with excellent static noise margin (SNM)

FinFET References

- C.Y. Chang, et al., “A 25-nm gate-length FinFET transistor module for 32nm node”, IEEE IEDM, Dec. 2009.
- C.-C. Yeh, et al., “A low operating voltage FinFET transistor module featuring scaled gate stack and strained engineering for 32/28nm SoC technology,” IEEE IEDM, Dec. 2010.
- C.C. Wu, et al., “High performance 22/20 nm FinFET CMOS devices with advanced high-k/metal gate scheme,” IEEE IEDM, Dec. 2010.