leti innovation for industry

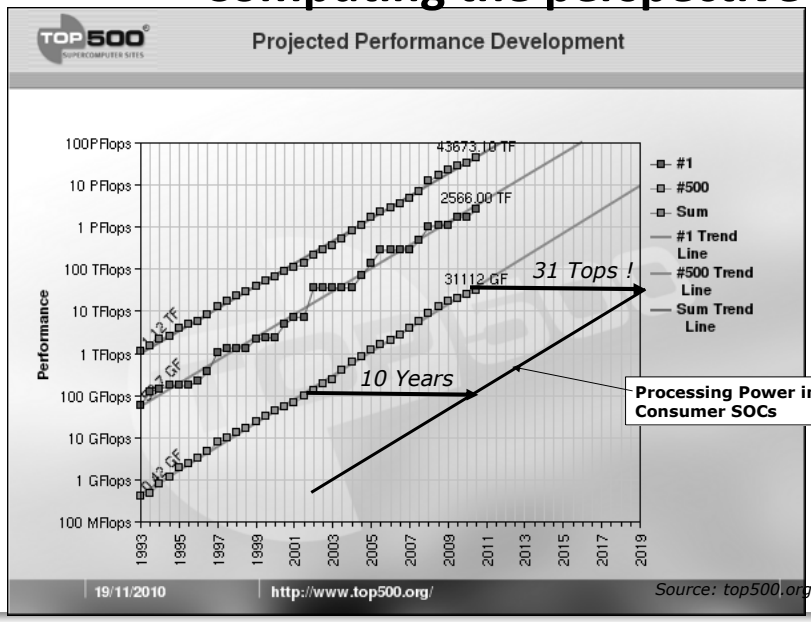
3D-IC for Computing

Ahmed Jerraya

Ahmed.jerraya@cea.fr

MINATEC CAMPUS

Computing the perspective



Source: top500.org

The Power challenge

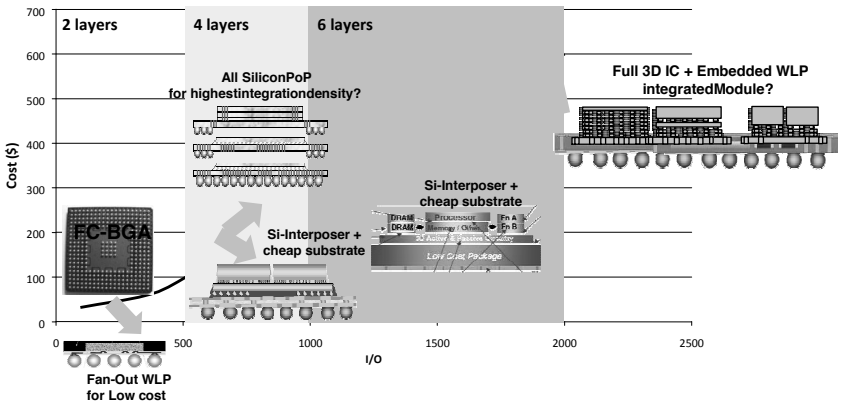
- Chips
  - 2009: CPU = 130 W (45 nm)
  - 2009: SoC Consumer 10W
  - 2009: SoC Mobile = 1 W
- HP Computers (Top 500)
  - 2009: 500mw/GFLOP wall
  - 2011: 1PFLOP = 1MW
  - 2016 : 1ExaFLOP= 1 GW (projection)

Rank	Computer	Cores	GFLOPS	Power KW
1	NUDT	186 368	2 566 000	4 040
2	Cray	224 162	1 759 000	6 950
3	Dawning	120 640	1 271 000	2 580
4	HP	73 278	1 192 000	1 398
5	Cray	153 408	1 054 000	2 910
6	Bull	138 368	1 050 000	4 590

leti *http://www.top500.org/*

The Packaging Challenge!

FC-BGA Package Cost Estimation *(Substrate + Bumping + Underfill+ Assembly)*



- FC-BGA substrate cost, complexity and thickness is increasing exponentially with number of chip I/O densities. To countercharge this non-acceptable trend:
  - Fan-Out WLP, Si interposers and combinations of both concepts will give birth to a new revival of the circuit assembly & packaging industry!

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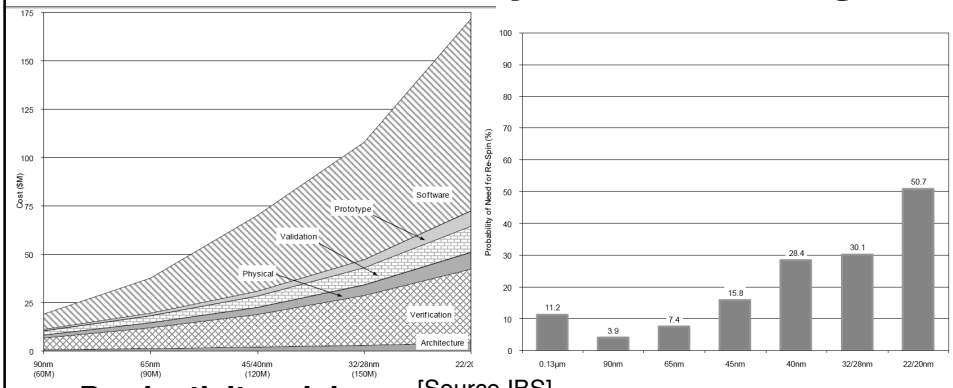
The cost and yield challenges

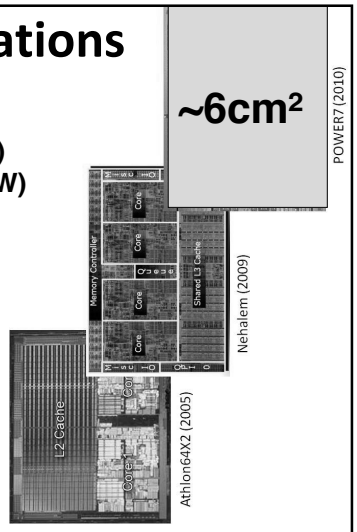


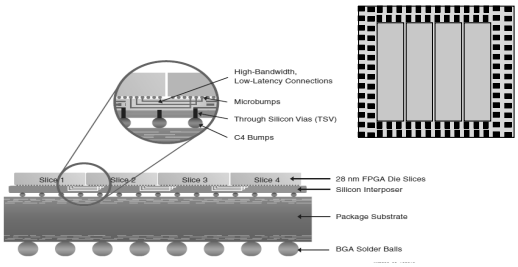
[Source IBS]

- **Productivity crisis**
  - **Design Cost is rocketing, 170M$ 22 nm**
- **Time to Market Crisis for**
  - **Design Respin rate reaching 50% for 22nm**

Implications

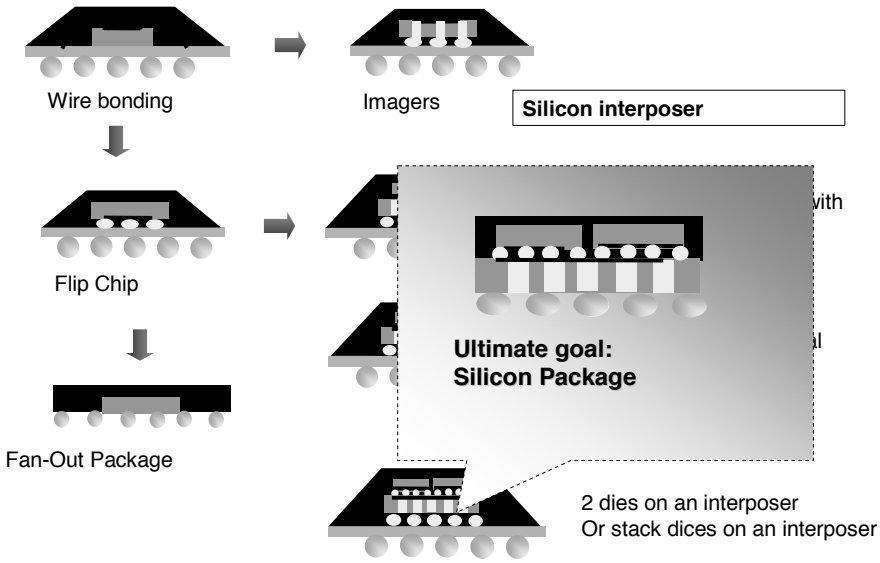
- **Main semiconductor manufacturing drivers**
  - **High performances IC (CPU, GPU, FPGA)**
  - **Maximum Integration on chip (6cm², 200W)**
- **The wall of Yield, cost, packaging … at 32-22nm**





3D-IC Prototype Xilinx 28 nm

3D packaging roadmap

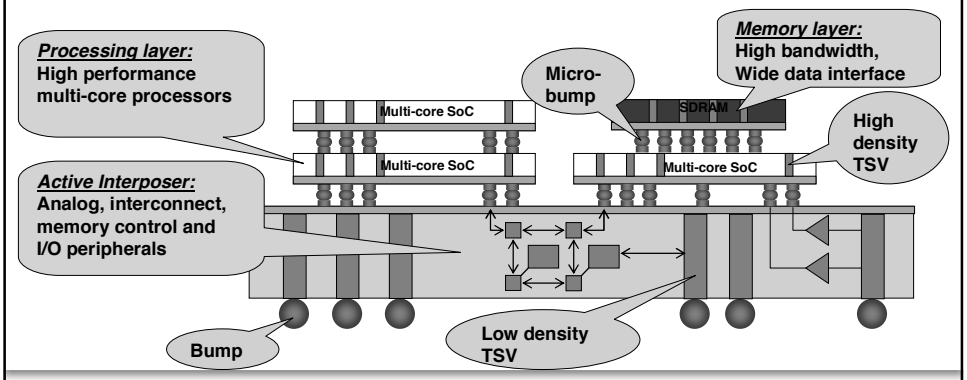


[N. Sillon LETI 2011]

Active Interposer Concept

- Heterogeneous integration rationale:
  - Digital logic shrinks significantly with process technology
  - Small dies shorten new process introduction and improve overall yield
  - Analog design and IOs doesn't shrink a lot with process technology
  - Short interconnect improves signal and power integrity

→ The SoC is partitioned into several dies, each of one being processed with the most relevant technology node in terms of performance and cost



3D design flow

Yesterday: Survivor kit…
- manual implementation of TSV
- Manual partitioning with 2D tools

More than 25 EDA companies Have R&D in Grenoble Area

Multiple partnerships to prepare 3D design flow

ATRENTA

3D Stack definition
- Multiple techno nodes
- Die partitioning
- Architecture exploration
- Simultaneous floorplan and TSV location exploration

DOCEA POWER

PRESTO Engineering

3D Stack/Package analysis & optimization
- Early floorplan & TSV Placement
- 3D Thermal Profile
- Test

Mentor Graphics

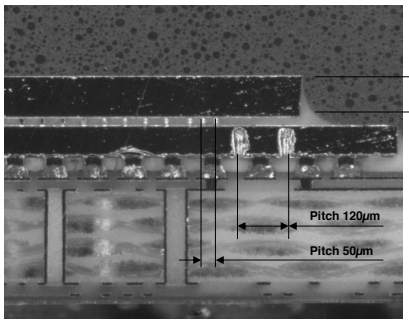
cadence

3D Implementation
- 3D Floorplan finishing
- Power planning
- 3D Routing with codesign
- 2D Place & CTS & Route
- 3D analysis (power/timing)

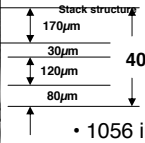
3D Active Si Interposer Demonstration

ST – LETI collaboration

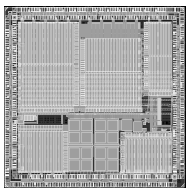
45nm technology stacked on 130nm interposer



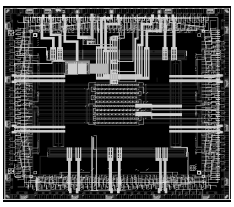
S. Cheramy, EMPC 2009



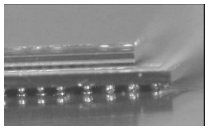
- 1056 inter-chip connections
- 588 TSV's
- 482 bumps
- BGA 864 balls, 1mm pitch



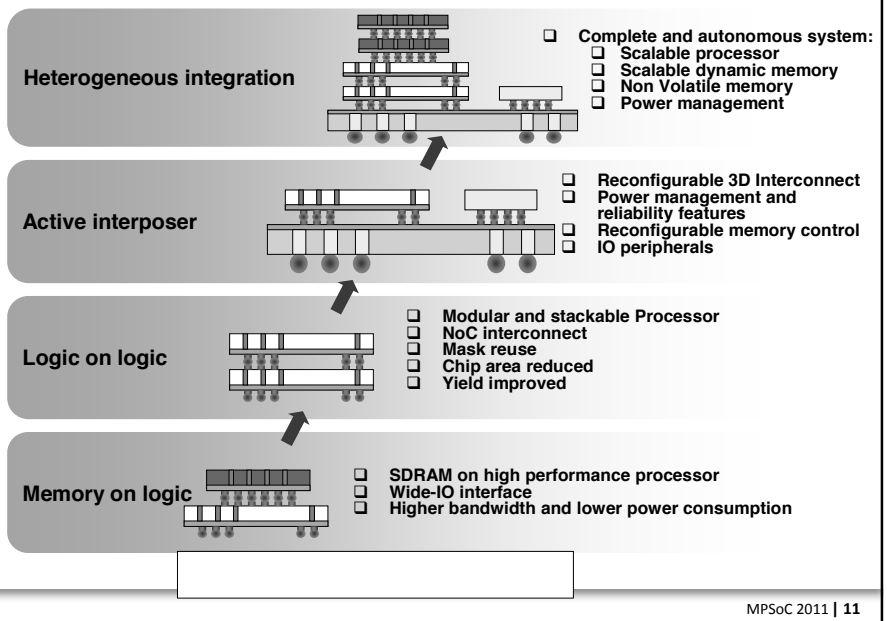
CMOS 45nm ,25 mm², 15Mb SRAM, ROM, std cells, …



Active interposer: CMOS 0.13µm, 32mm²



Leti's 3D-IC ongoing demonstrators



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leti
LABORATOIRE D'ÉLECTRONIQUE
ET DE TECHNOLOGIES
DE L'INFORMATION
CEA-Leti
MINATEC Campus, 17 rue des Martyrs
38054 GRENOBLE Cedex 9
Tel. +33 4 38 78 36 25
www.leti.fr
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MINATEC
INSTITUT
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