Fine grain DVFS power-aware control

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MPSoC 2011, Beaune

- Objective ▸ An ***Adaptive*** Voltage and Frequency scaling approach at ***fine grain*** to reach a functional optimal ***energetic*** point according to ***PVT variations***

- Context Reminder
- GALS NoC Architectures
- Adaptive Architectures
- MPSoC fine-grain power control
- Our Fine-grain AVFS proposal

Context Reminder

Cost, area, power consumption issues and increasing performances

Lead to

Nanometric transistor design | **Low power architectures**

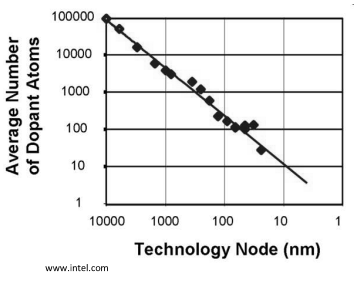
Limited by

Transistor fabrication difficulties
Physical Limits
Increasing IC complexity

Increasing Process and Environmental Variability

Context Reminder

- PVT variations with very different spatial and temporal dynamics
  - Process
  - Voltage
  - Temperature



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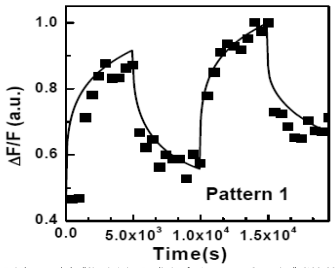
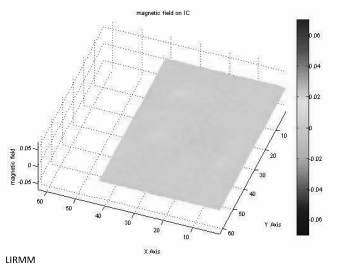
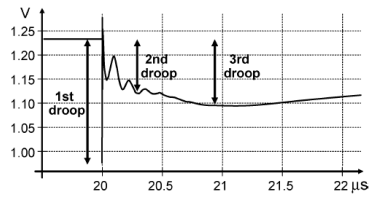


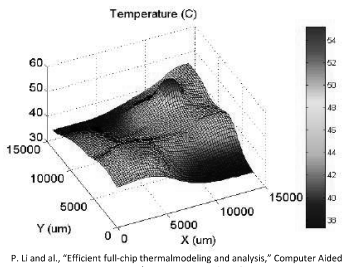
Rui Zheng and al. , "Circuit Aging Prediction for Low-Power Operation", CICC, 2009



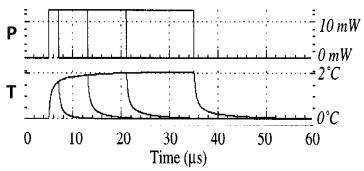
LIRMM



Keng L. Wong and al., "Enhancing Microprocessor Immunity to Power Supply Noise With Clock-Data Compensation", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 4, APRIL 2006

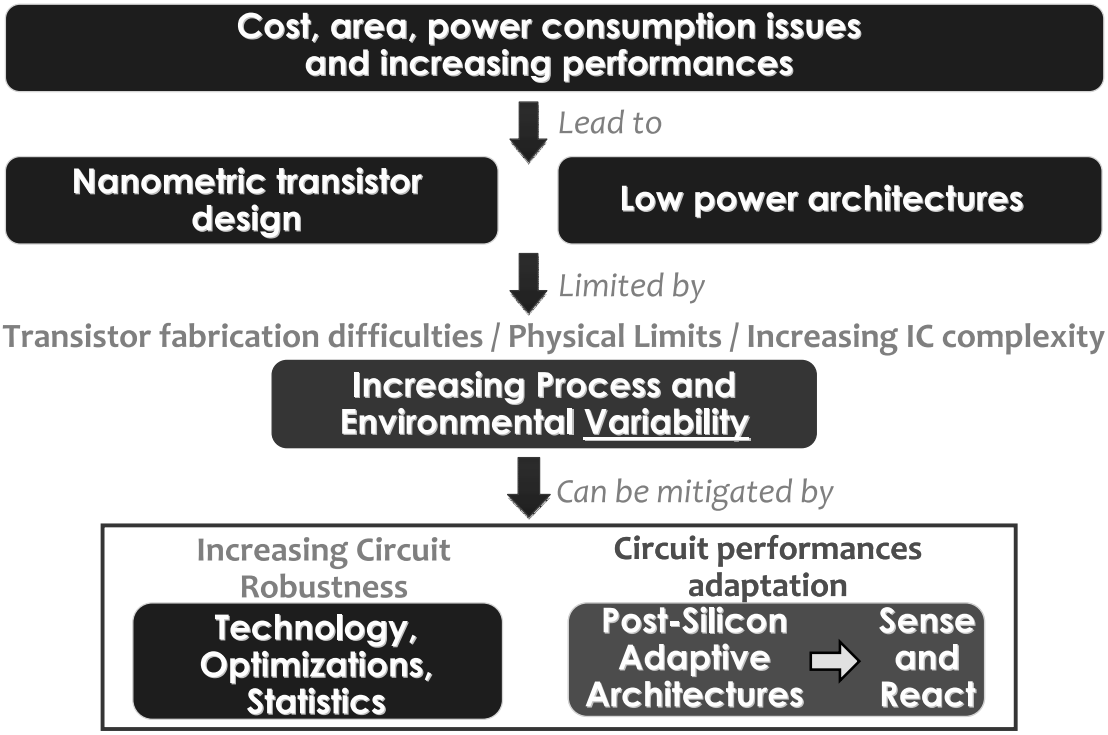


P. Li and al., "Efficient full-chip thermalmodeling and analysis," Computer Aided Design, 2004. ICCAD-2004.IEEE/ACM International Conference on, pp. 319–326, 2004.



J. Altet and al., "Thermal couplingin integrated circuits: application to thermal testing," Solid-StateCircuits, IEEE Journal of, vol. 36, pp. 81–91, 2001.

Context reminder



GALS NoC architectures

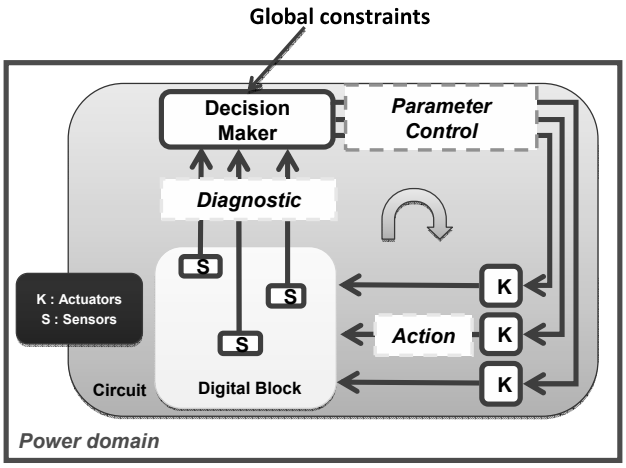
- Main innovations based on GALS architectures (Globally Asynchronous and Locally Synchronous NoC since 2002
  - Based on a strong knowledge on asynchronous QDI circuits
- A basic architecture for a simple, efficient and low power clock distribution
- A natural enabler for a fine grain dynamic power management :
  - Easy frequency scaling (independant frequency islands)
  - Fine grain voltage and Vt management (independant voltage and frequency islands)
- An essential architecture for PVT variations to avoid worst case design :
  - Fine grain adaptive architecture (local V/F point adapted to dynamic PVT variations)
  - Asynchronous QDI robustness to variations

=> One unique target : Reach an optimum functionnal point at a maximum speed for a minimum energy considering local, global and environmental variations

Adaptive architectures

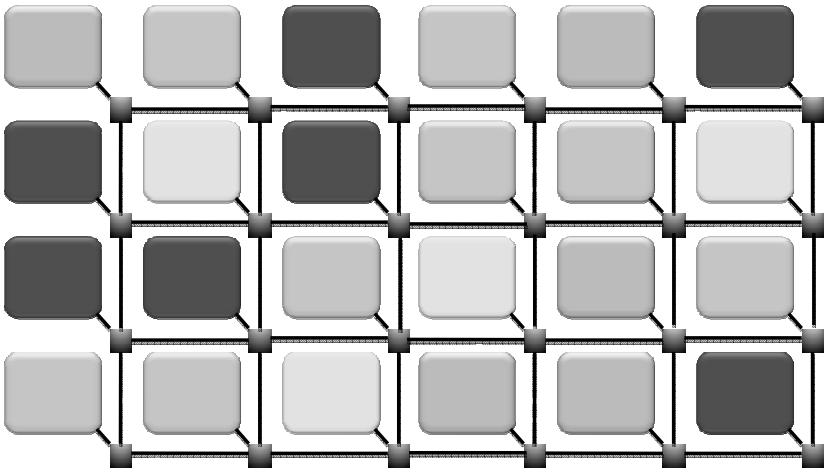
- A dynamic adaptive architecture to allow circuit performances regulation :
  - Improve circuit performance (power, speed)
  - Improve the yield
- We need to :
  - Know the real **process corner case**
  - **Dynamically** follow the temperature, voltage and aging evolution

  ⇒ Find an **optimum functional point** avoiding important design margins



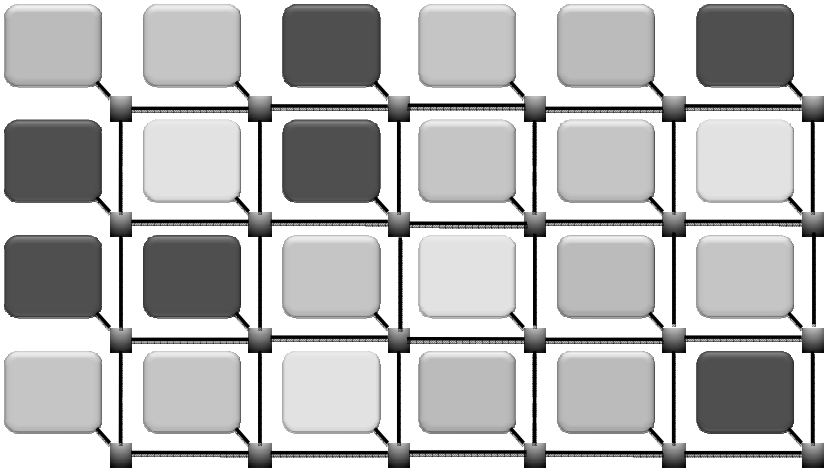
MPSoC fine-grain power control

- On-chip Process variations



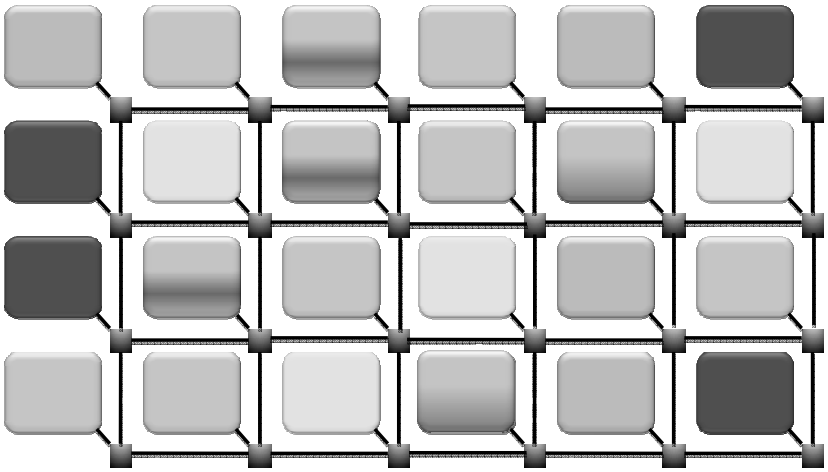
MPSoC fine-grain power control

- Dynamic PVT evolution



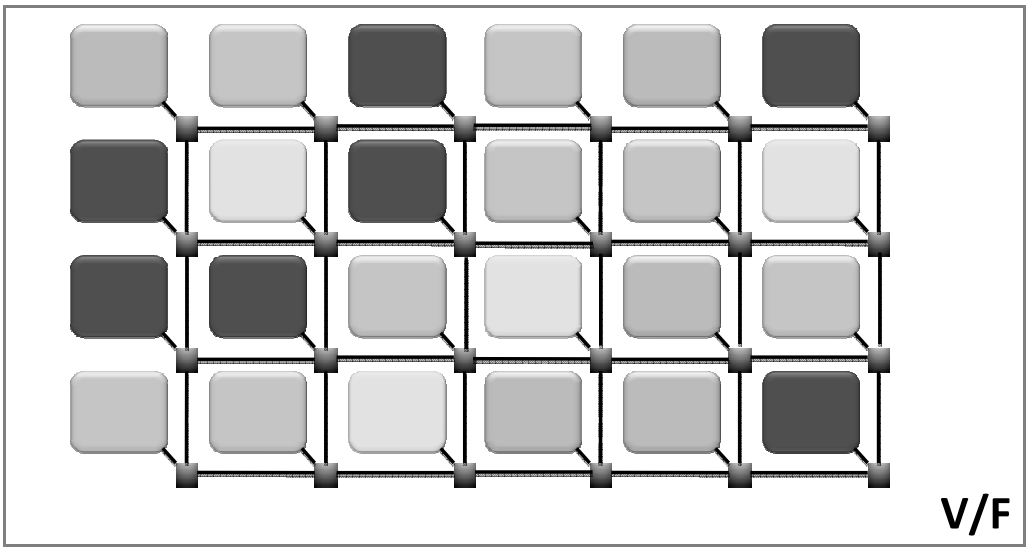
MPSoC fine-grain power control

- Unbalanced workload according to application



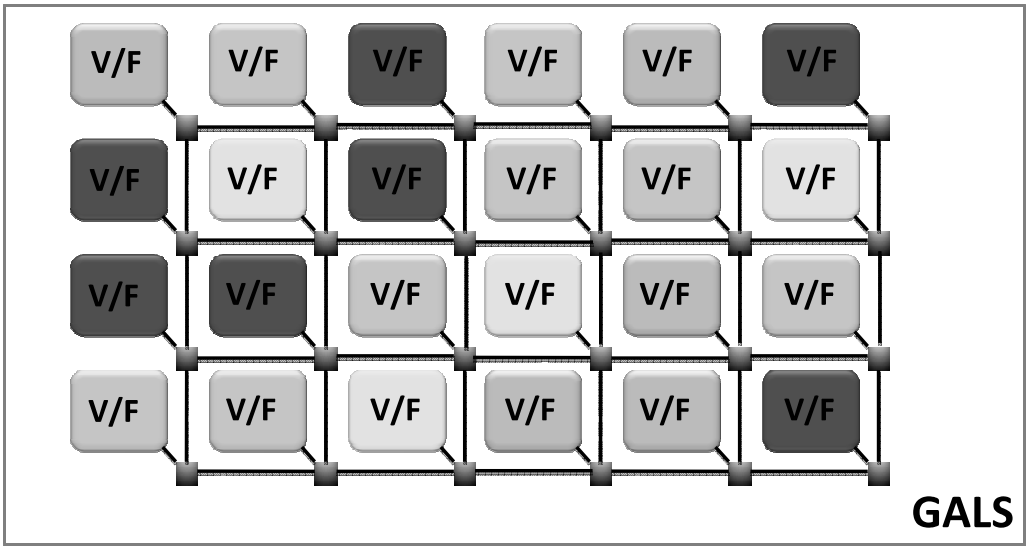
MPSoC fine-grain power control

- What about a worst case approach : unique V/F point ?



MPSoC fine-grain power control

- Adpative fine grain approach for maximum energy gain and efficiency



Adaptive architecture

Hardware platform considered :

- LoCoMoTIV* hardware platform developed by CEA-LETI Minatec
  - A 32nm STMicroelectronics technology demonstrator for fine grain Local Dynamic Adaptive Voltage and Frequency Scaling
  - GALS Architecture

- Sense and React architecture :
  - Sensors
    - Process-Voltage-Temperature
    - Timing fault
  - Actuators
    - Local supply voltage generation (V) using Vdd-hopping
    - Local clock generation (F) using low area FLL
  - Power/Variability Control
    - Local control with minimum hardware
    - Global control : high level algorithms

E. Beigné and H. Metras, "A Dynamically adaptive multiprocessor architecture addressing advanced CMOS technology variability", ESC conference, May 2-5 2011

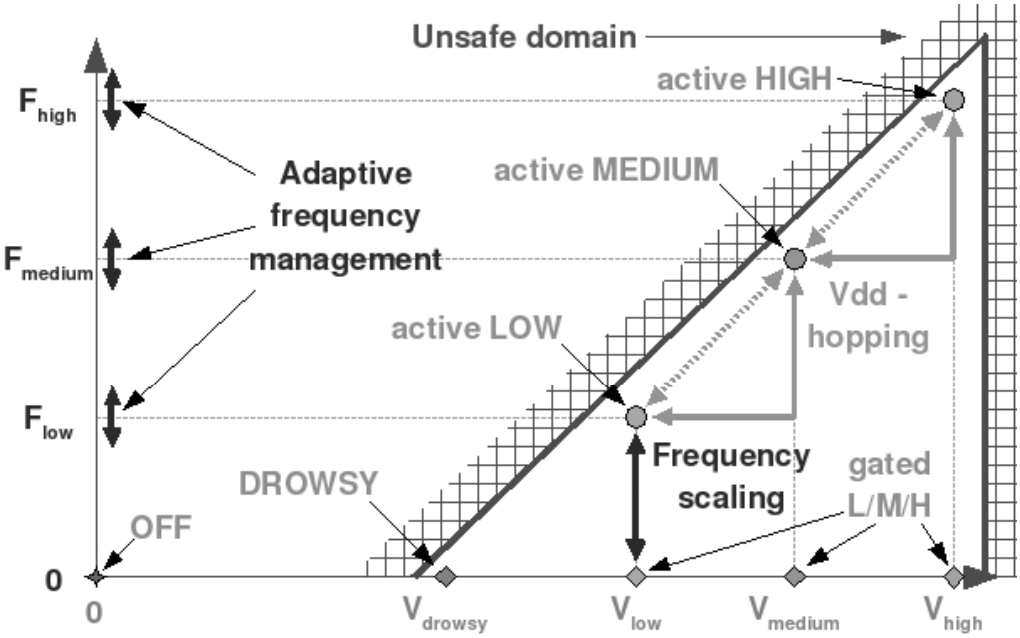
* Local Compensation of Modern Technology Induced Variability

Domains main characteristics

- Each domain is an independant power and frequency domain :
  - a GALS scheme within the cluster
  - domains are synchronous islands using programmable clock generator
  - Within each domain, the logic core is supplied by *Vcore* voltage generated from the external available voltages : Vhigh/Vmedium/Vlow/Vdrowsy
  - Dynamic variability monitoring

➢ Local fine grain power and variability management can be executed during IP computation and communication independently from the others

Power domain 'power modes'



Area/Power/performance budget

- Considering a Power Domain of about 0,75 mm² in 32 nm running at 600 MHz
- For an area overhead of ~10% we can obtain from 20% to 80% of dynamic power consumption reduction depending on :
  - Intrinsic variability
  - Workload balancing
- Allow to find a functionnal point (V/F) even at low speed whatever is the process variation

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Thank you for your attention

Actuators

Vdd Hopping Power Supply Unit

- Power Supply Unit manages internal *Vcore :*
  - Two fixed voltages available : Vhigh/Vlow
  - Hop between those two values using a dithering ratio
- Two power switches *Thigh* and *Tlow* LVT transistors
- A Hopping Unit (for fine grain AVFS at IP level)

LPM : Local Power Manager
LCG : Local Clock Generator