
# Innovation Trends in Image Sensor Technologies

Yosuke Ueno
2025.06.16 MPSoC2025


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# Outline

- **Image sensor technology**

  **- Evolution of stacked device integration**

- **Combination with sensing technology**

  **- Combination with Event-based vision sensor (EVS)**

  **- Combination with SPAD to Quanta image sensor (QIS)**


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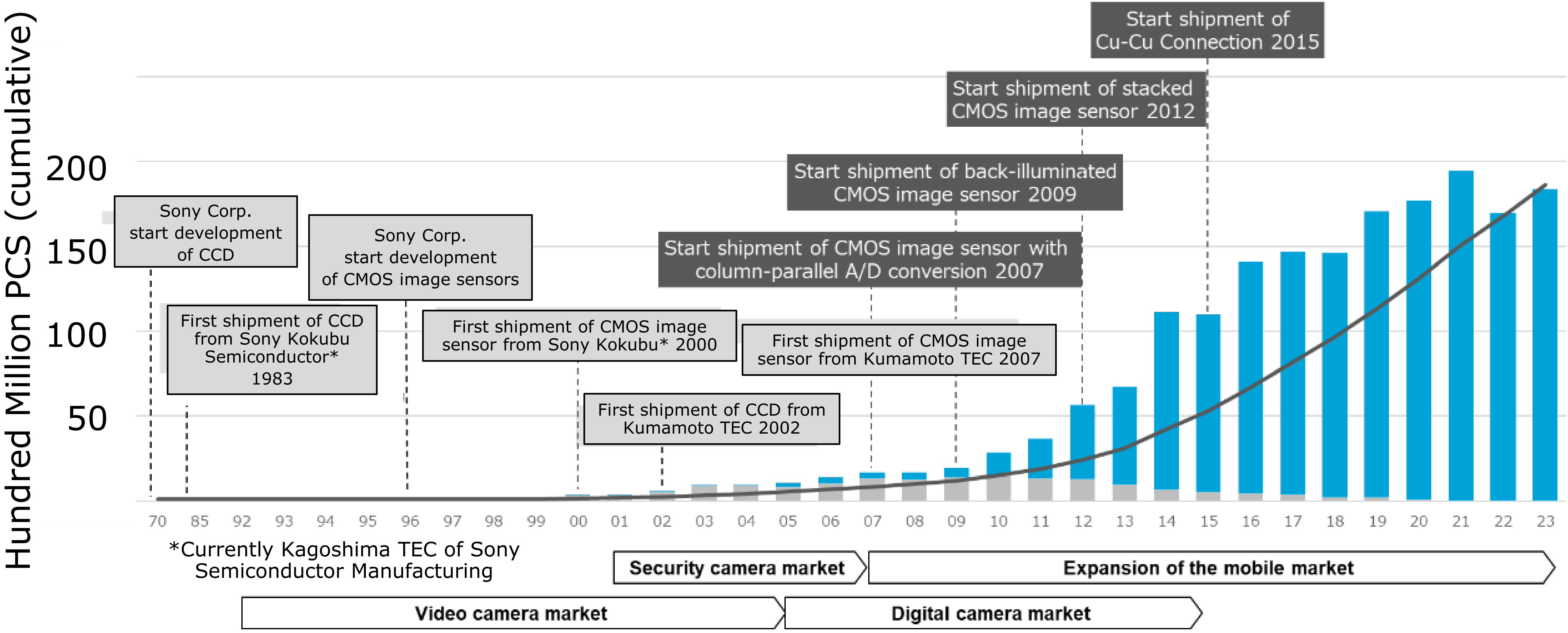
# Sony CCD and CMOS Image Sensors trend and milestones





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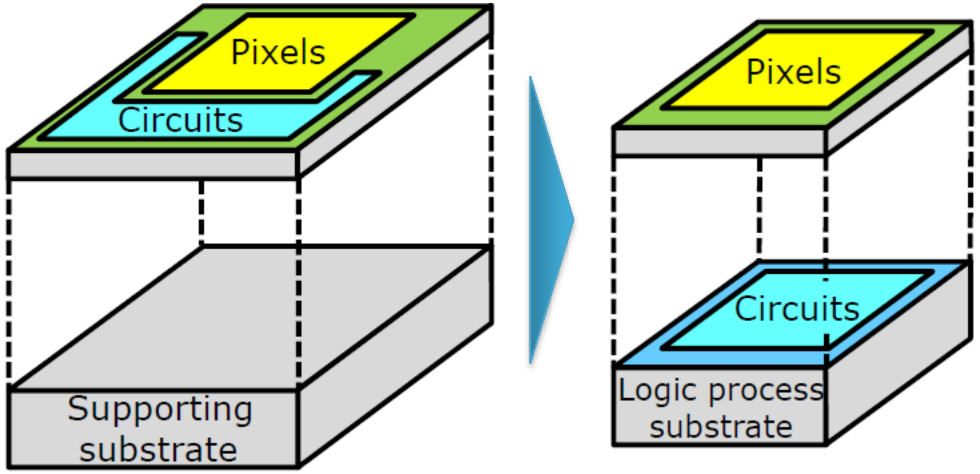
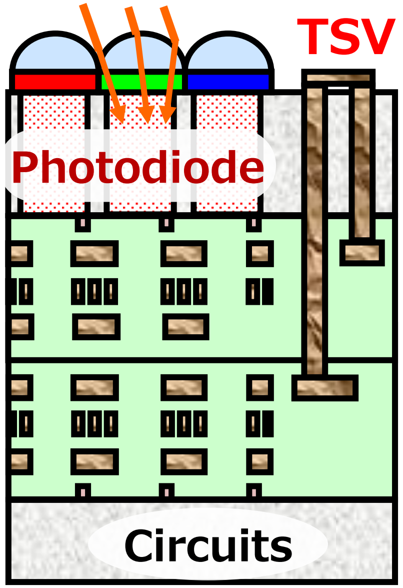
# Introduction of 1st Stacked CIS

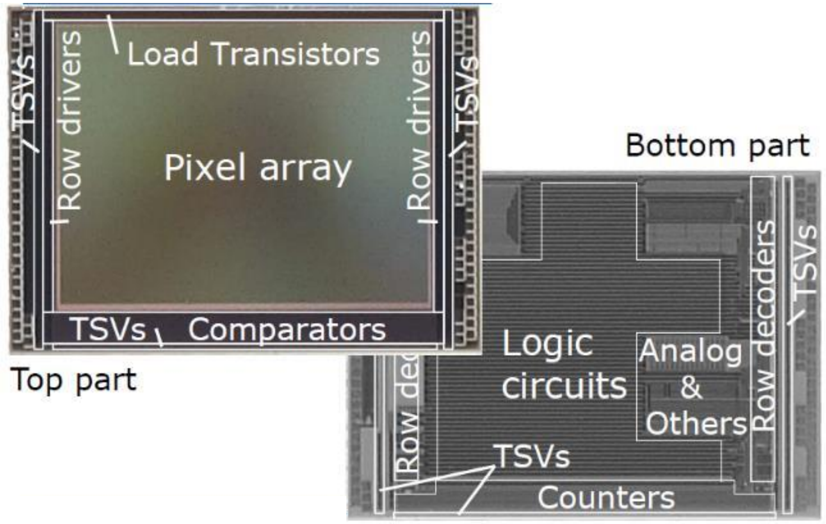
**Stacked CIS has become mainstream in mobile cameras.**
**Evolving into compact and highly functional imaging.**

Back-illuminated CIS

Back-illuminated **Stacked** CIS




S. Sukegawa, ISSCC 2013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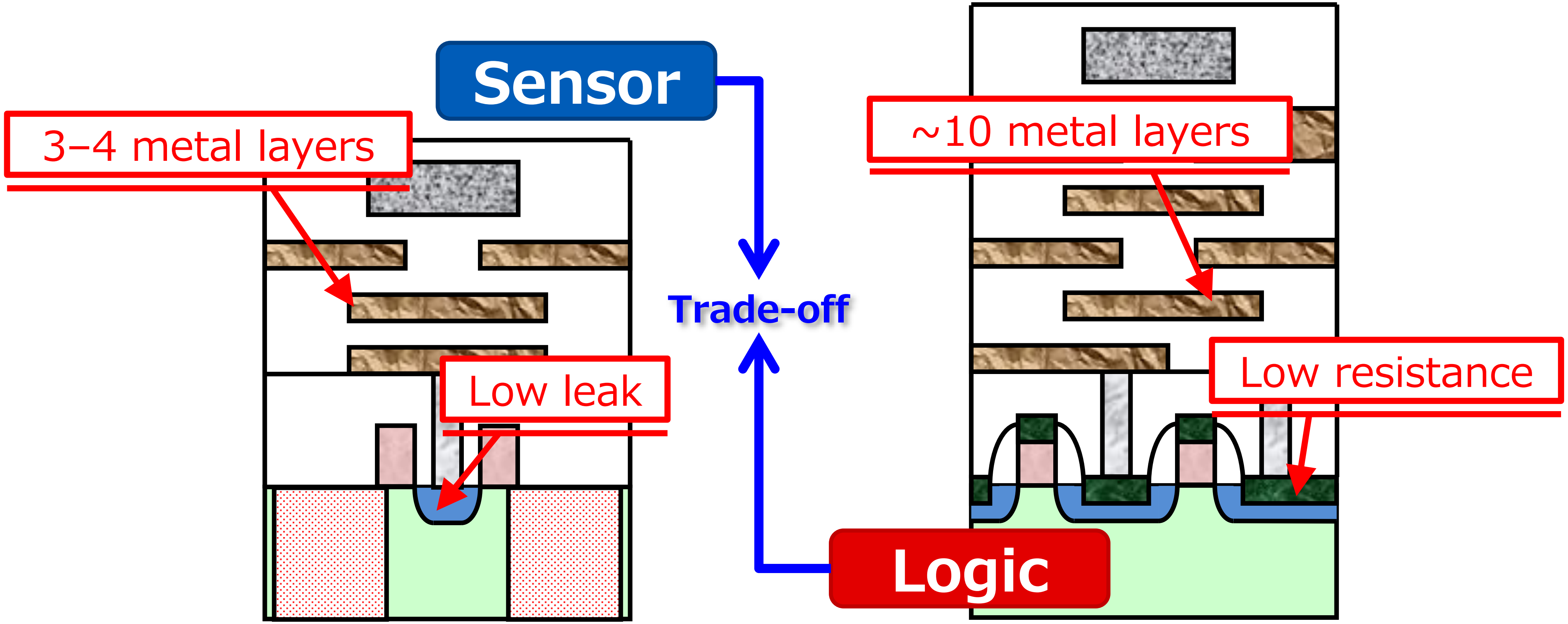
# Why is Stacked CMOS Image Sensor Effective?

**Optimal process technologies differ from sensor to logic.**
**3D stacking technology can relax the constraint.**





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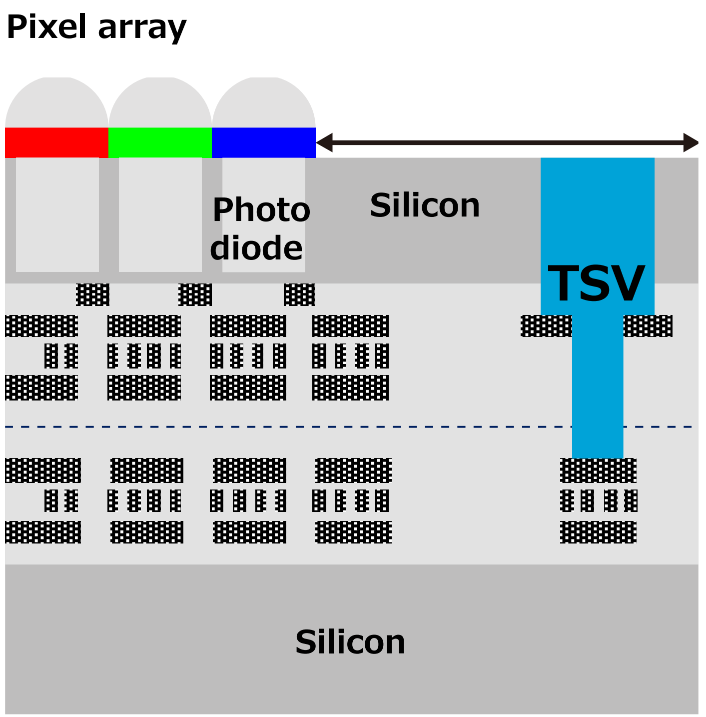
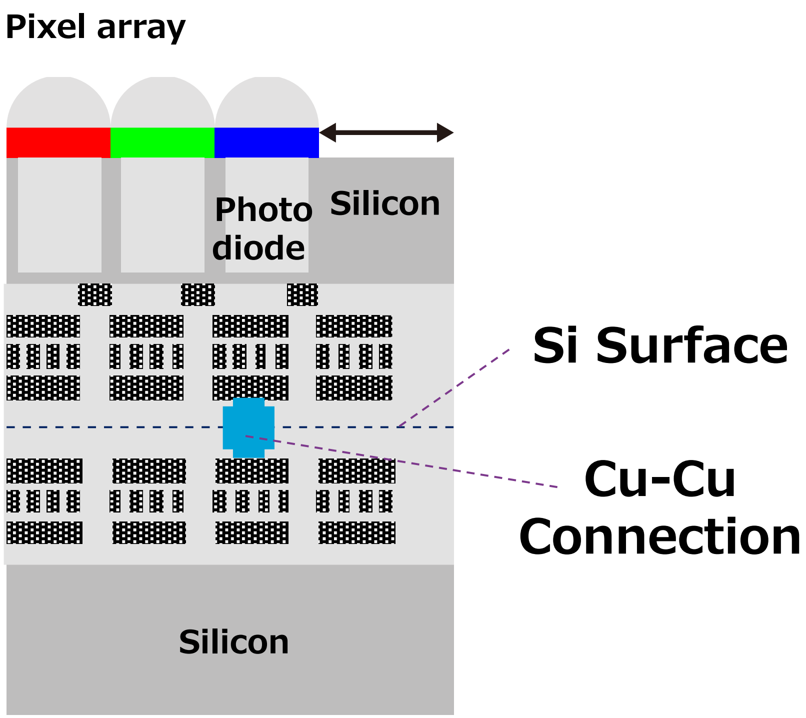
# Evolution in Bonding

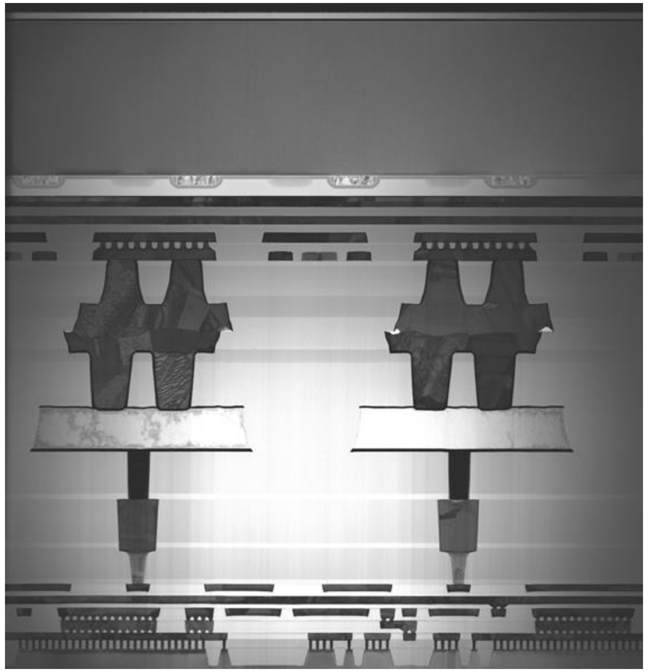
## Hybrid Bonding (Cu-Cu connection) mass-produced since 2015.

**TSV Connection**
**(Conventional)**

**Cu-Cu Connection**



Y. Kagawa et al., IEDM 2016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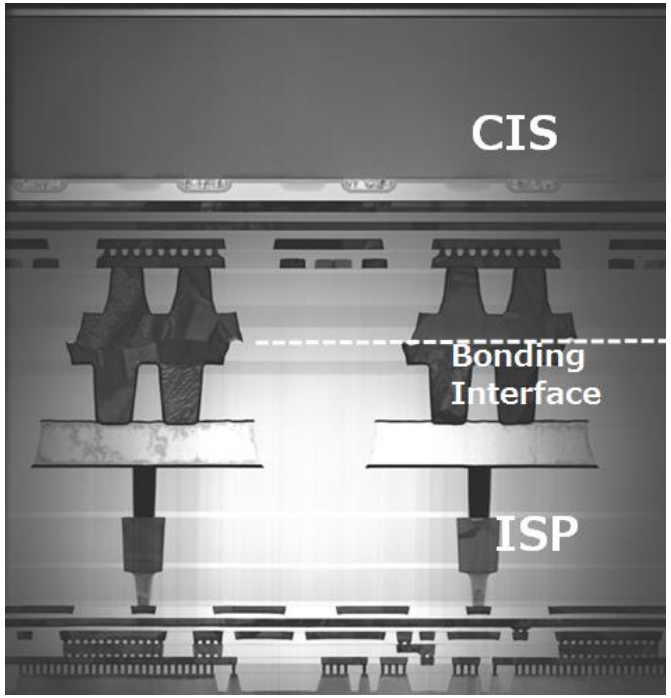
# Trend of Cu-Cu Connection Pitch

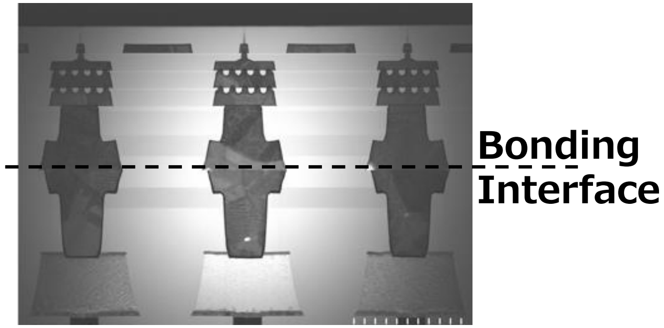
**Cu-Cu connection pitch is further being reduced to enable pixel-parallel architecture.**

**6μm pitch**



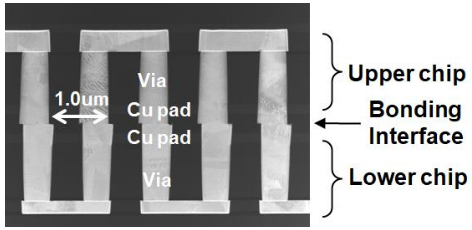

**2016**

**3μm pitch**




**2019**

**1μm pitch**




**2020**

Y. Kagawa, EDTM 2016
Y. Kagawa, IITC 2020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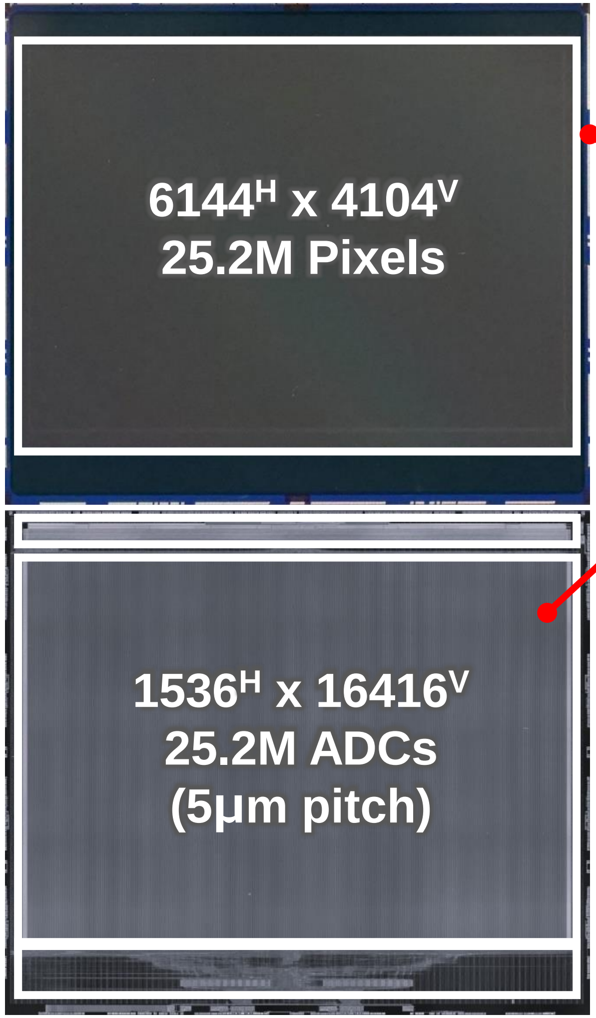
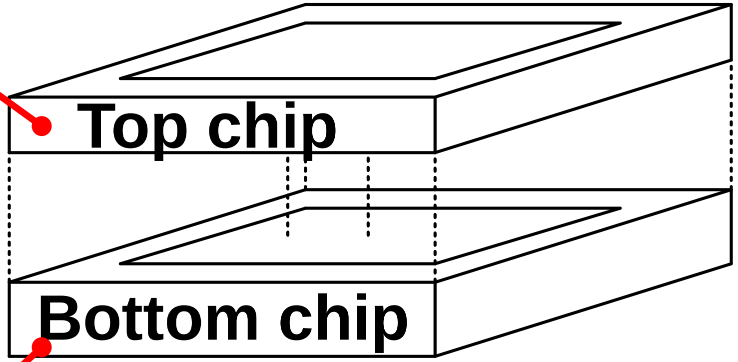
# Cu-Cu Connections for Pixel Parallel Readout

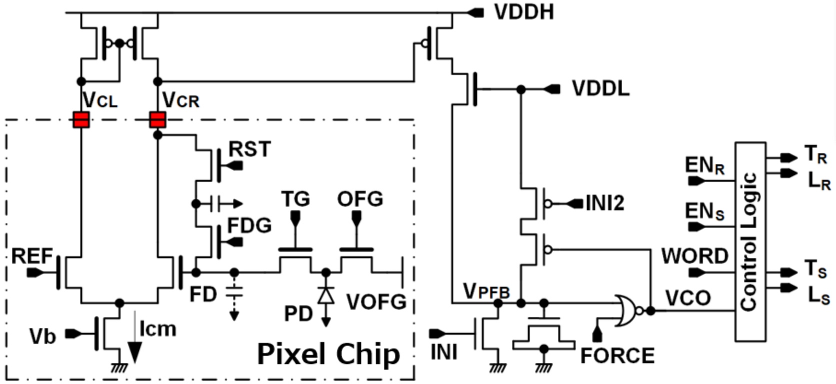
**Pixel parallel data output can realize high-speed distortion-free Image.**




## Cu-Cu Connection




## Circuit diagram




**Capture: 120 fps, Play: 15 fps**

T. Kainuma, ISSCC 2025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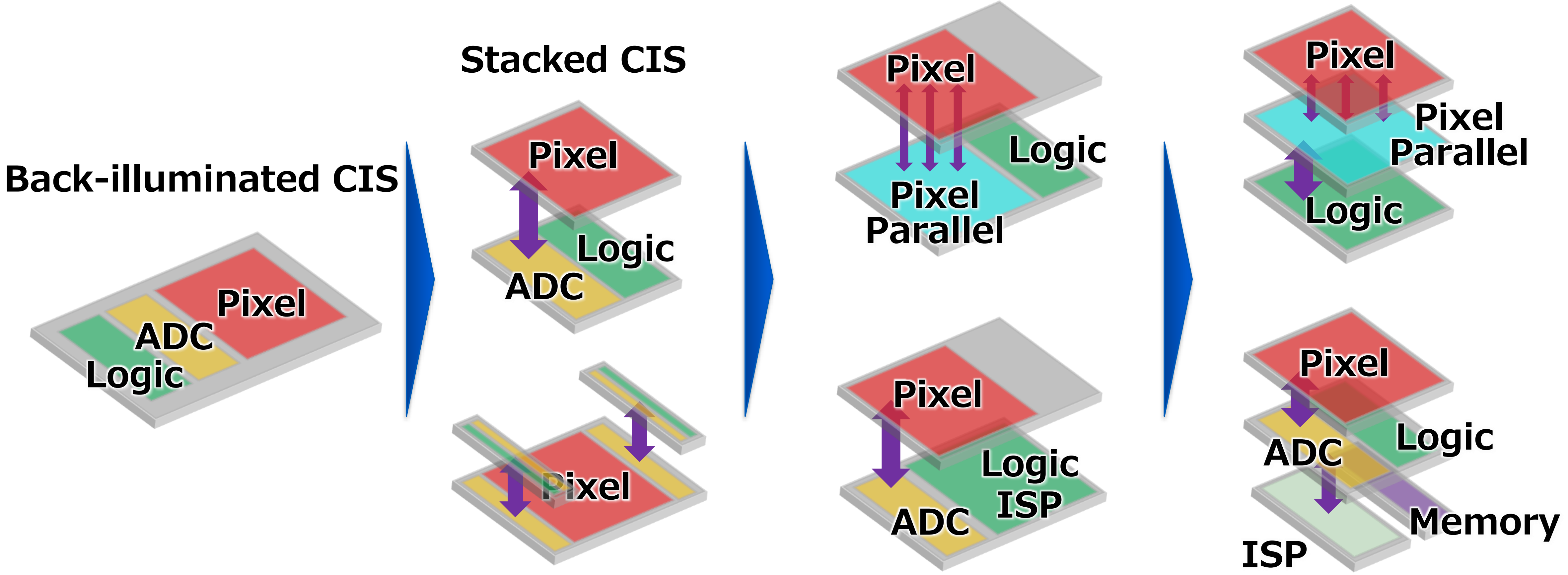
# Technology Trends – Evolution of Stacked Device Integration

**Evolution of stacked device integration accelerates to integrate imaging and sensing technologies.**





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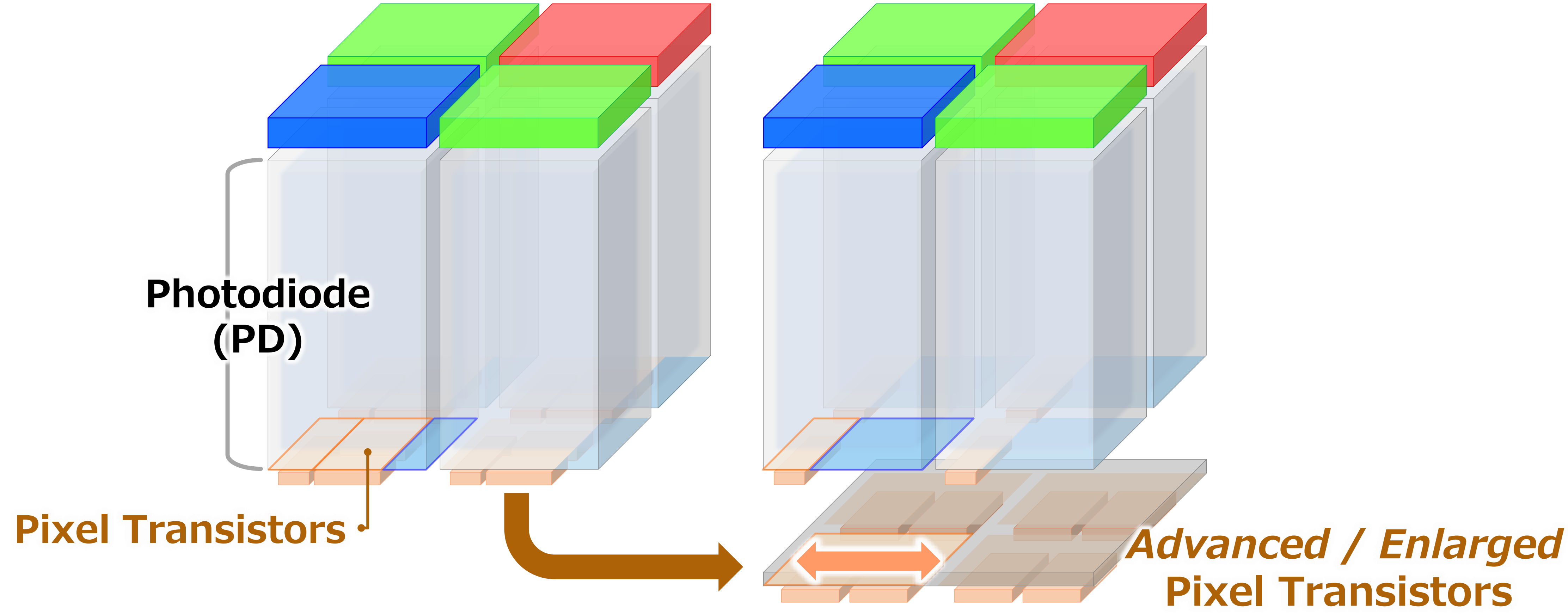
# Further Evolution of Stacked CMOS Image Sensor for Mobile

## 2-Layer Transistor Pixel splits Si layers for PD and pixel transistors.





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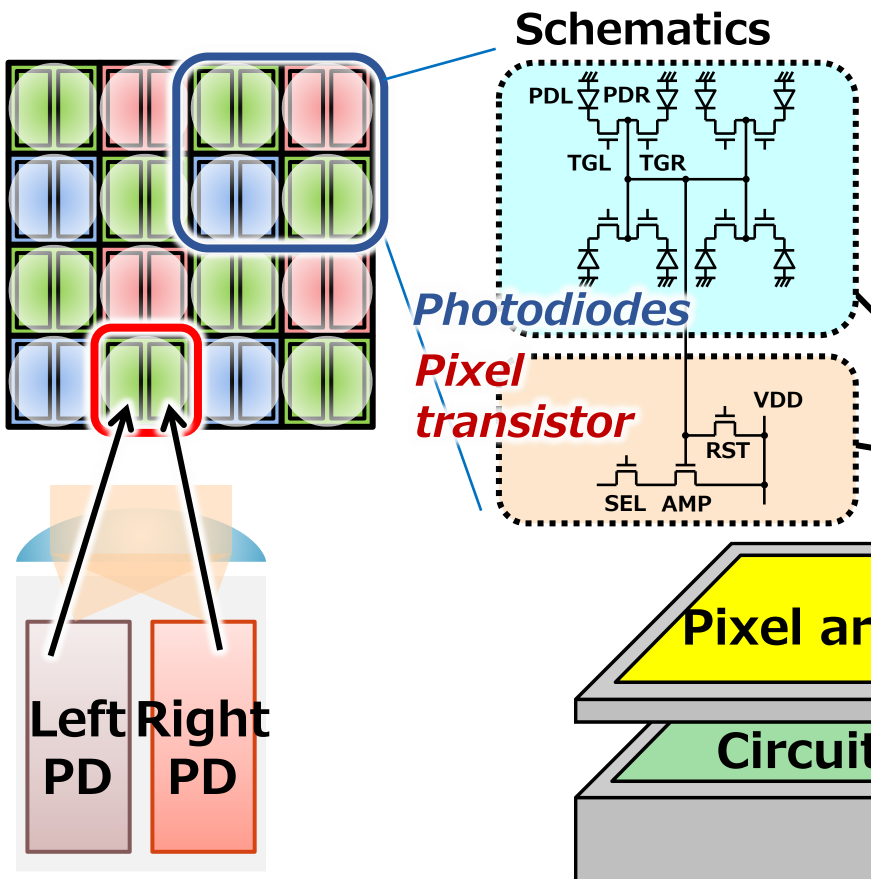
# Further Evolution of Stacked CMOS Image Sensor for Mobile

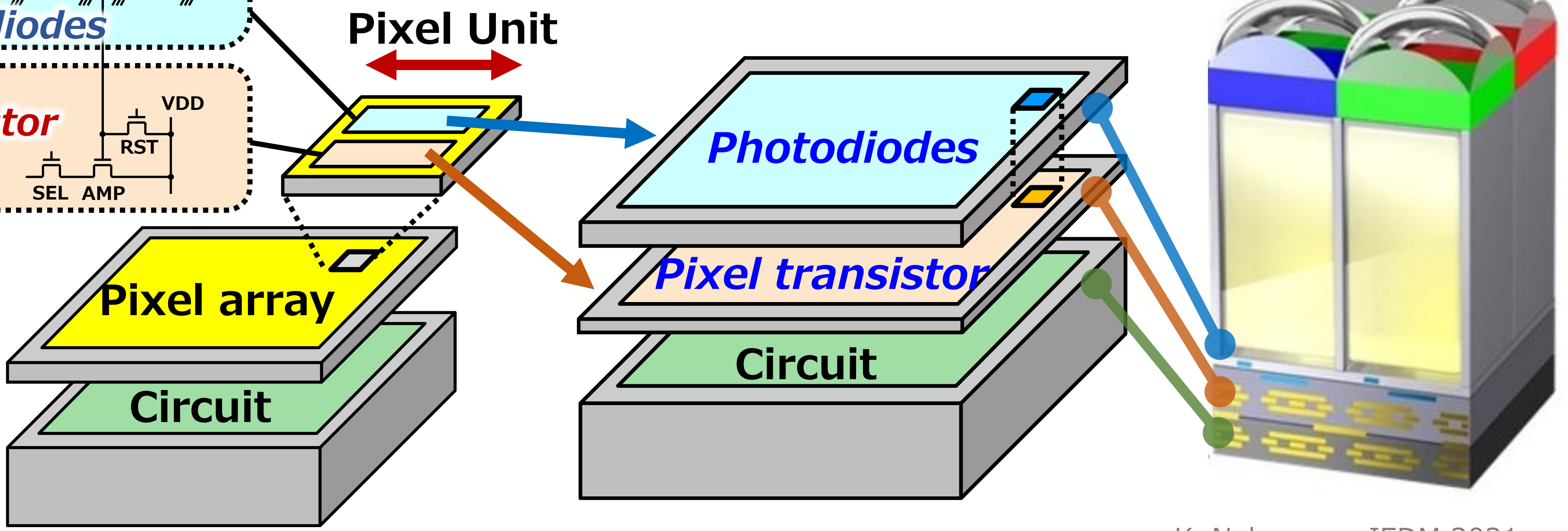
## 2-Layer Transistor Pixel improves image characteristic (FWC/Noise).

- ✓ **High FWC** owing to large PD volume
- ✓ **Low noise** owing to large pixel transistors




Dual PD for autofocus

M. Kobayashi, IISW 2015




K. Nakazawa, IEDM 2021
K. Zaitsu, VLSI Symp. 2022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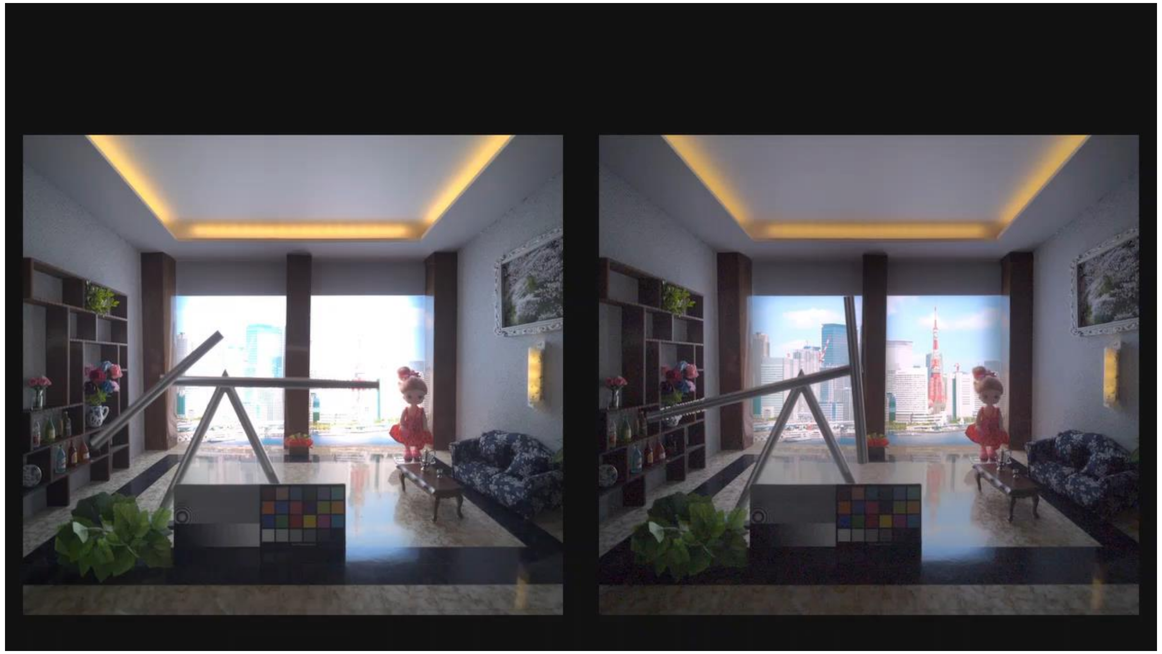
# Improved Video Performance by 2-Layer Transistor Pixel

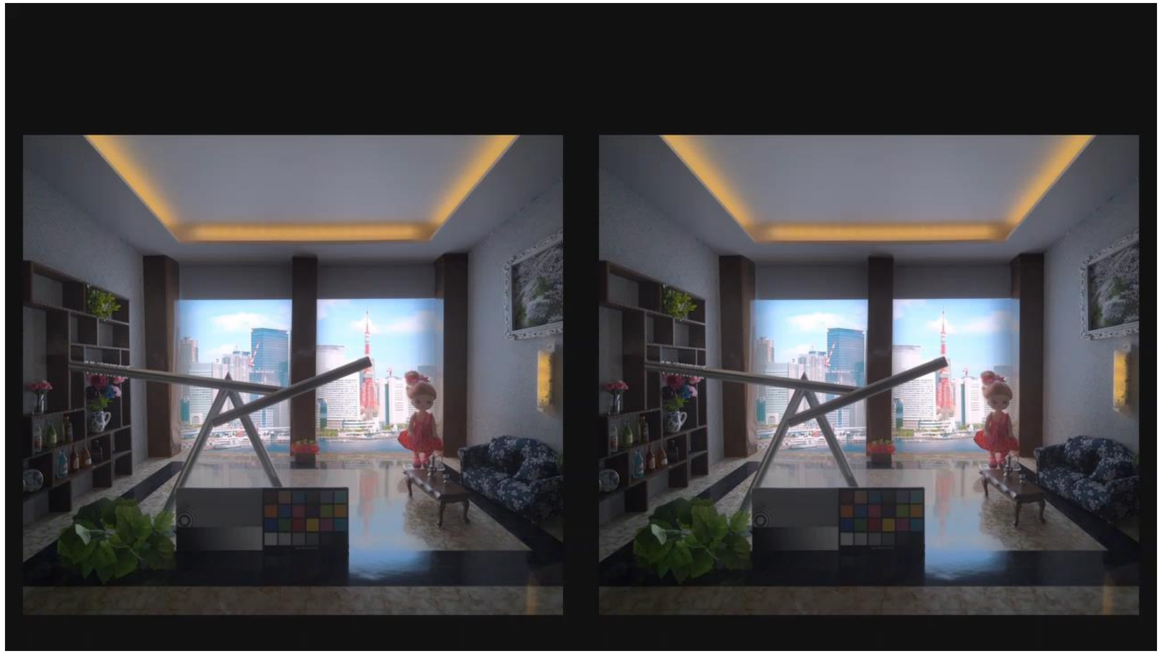
## Improved by expanding the dynamic range in a single frame.

### Conventional Pixel



When shooting video,
HDR with multi-frame processing is not possible.
Trade-off between dark noise and bright saturation.

### 2-Layer Transistor Pixel



By realizing noise reduction and saturation expansion,
clear videos in both brightness and darkness are available.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  - Combination with SPAD to Quanta image sensor (QIS)


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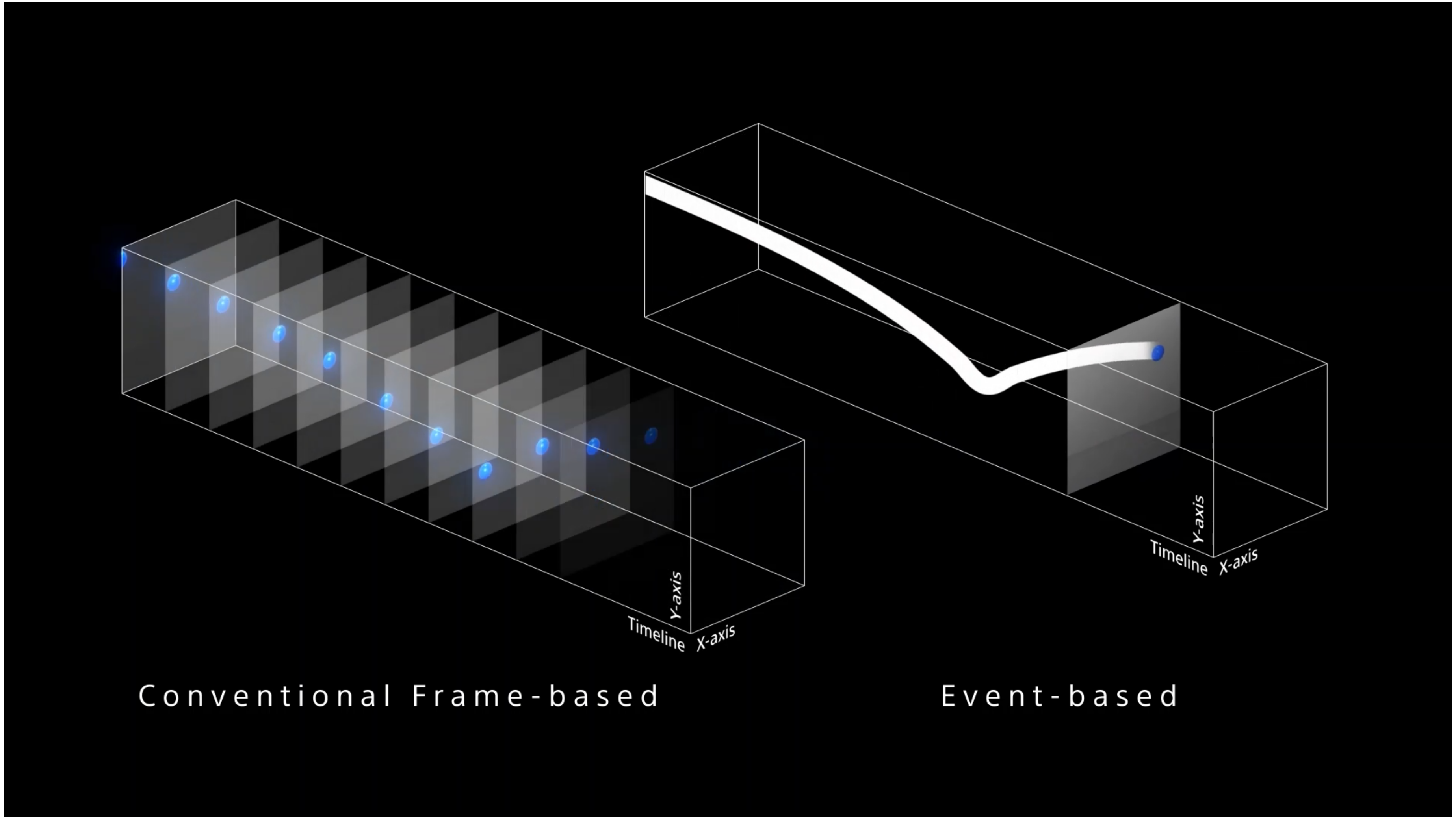
# Event-based Vision Sensor (EVS)

**Every pixel asynchronously detects contrast change of light.**





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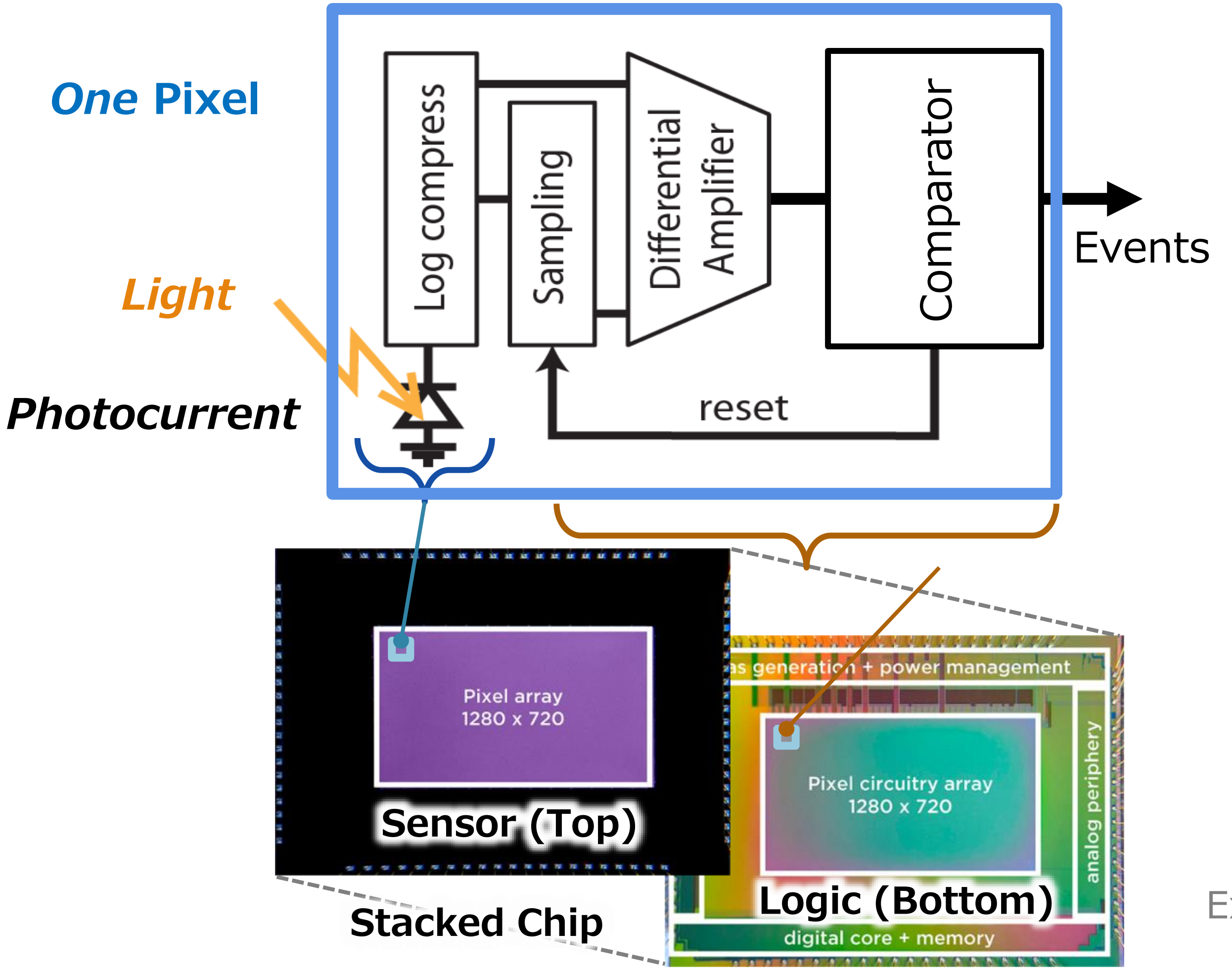
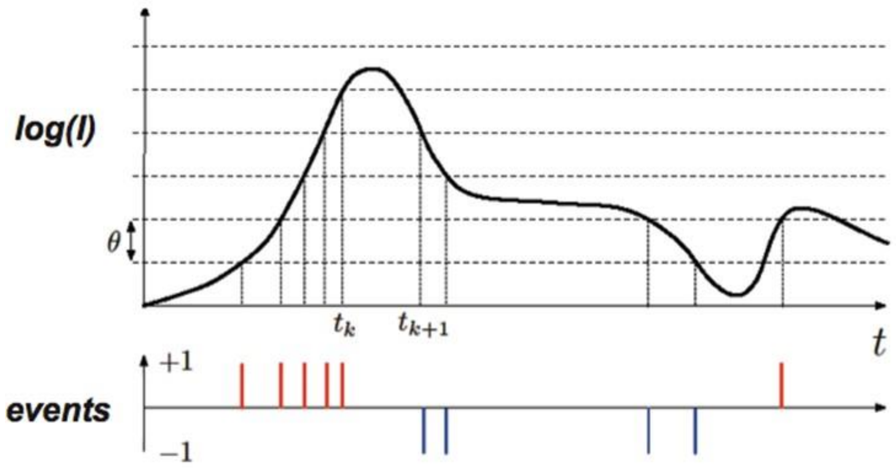
# Event-based Vision Sensor (EVS)

**Event detection circuits implemented in pixel parallel.**

## Pixel Circuitry




## Photocurrent (Incident intensity)




Ex) T. Finateu, ISSCC 2020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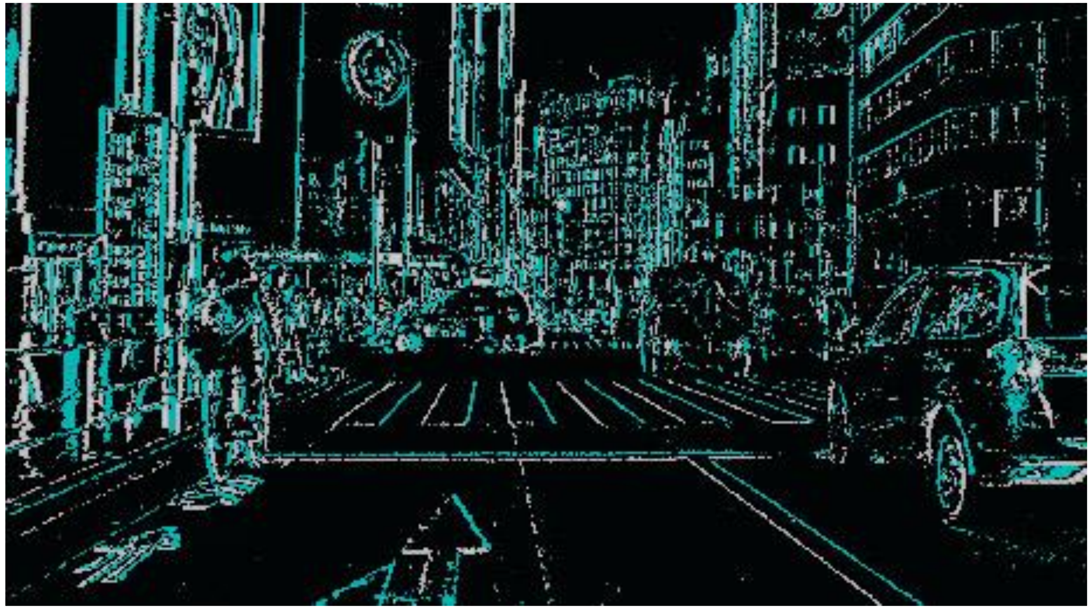
# Output of Event-based Vision Sensor (EVS)

**Only pixels with positive/negative contrast change generate data.**

**Standard Color Sensor**

**Event-based Vision Sensor (EVS)**



**Blue** : *positive* contrast change
**White** : *negative* contrast change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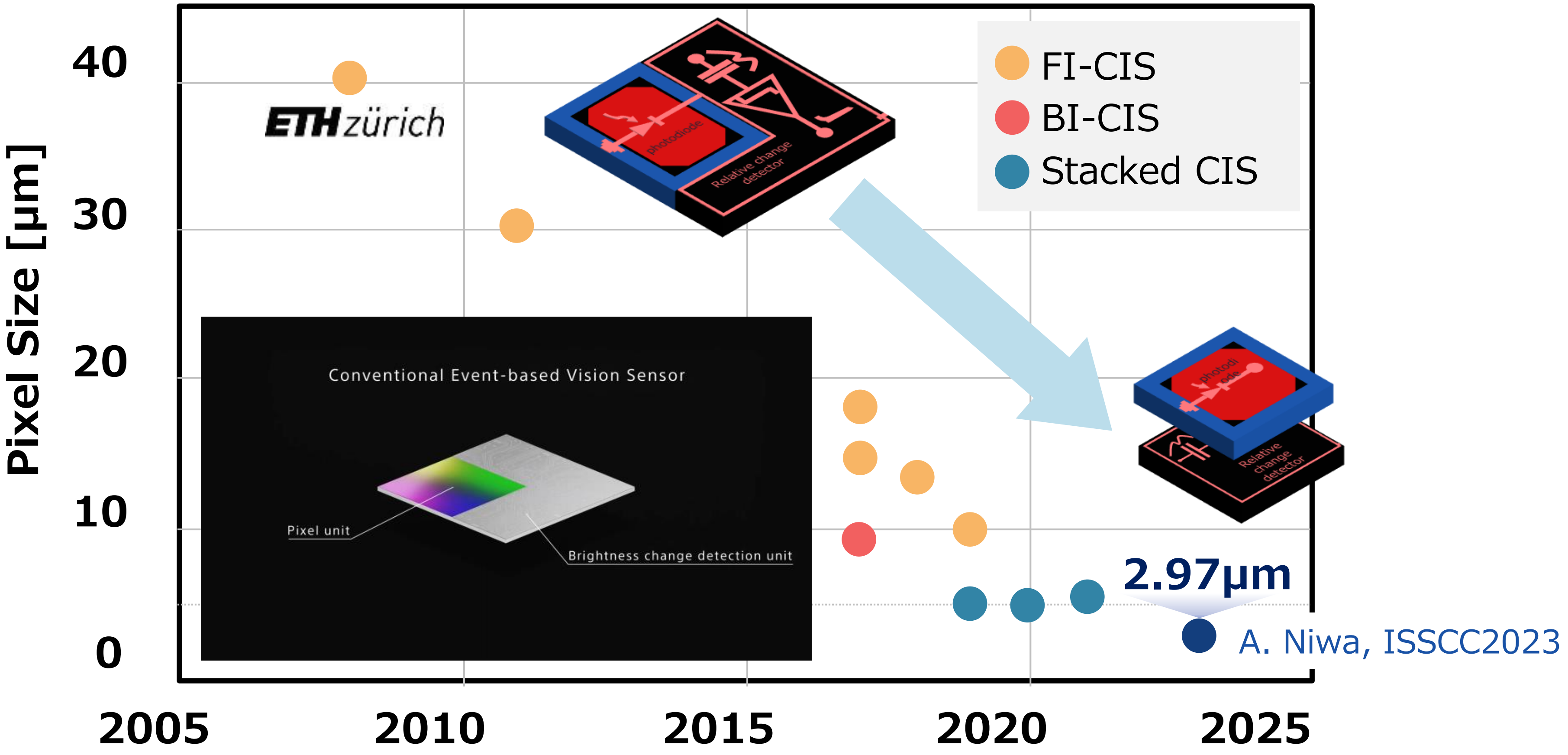
# Trend of Event-based Vision Sensor

**Smaller pixel pitch using pixel-parallel stacked connection.**





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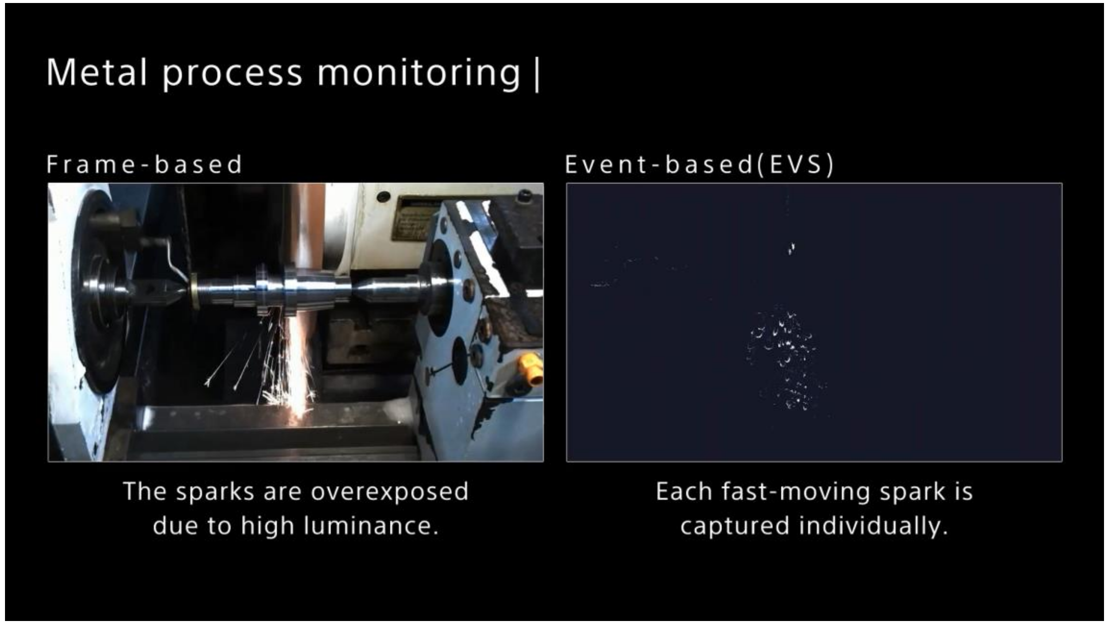
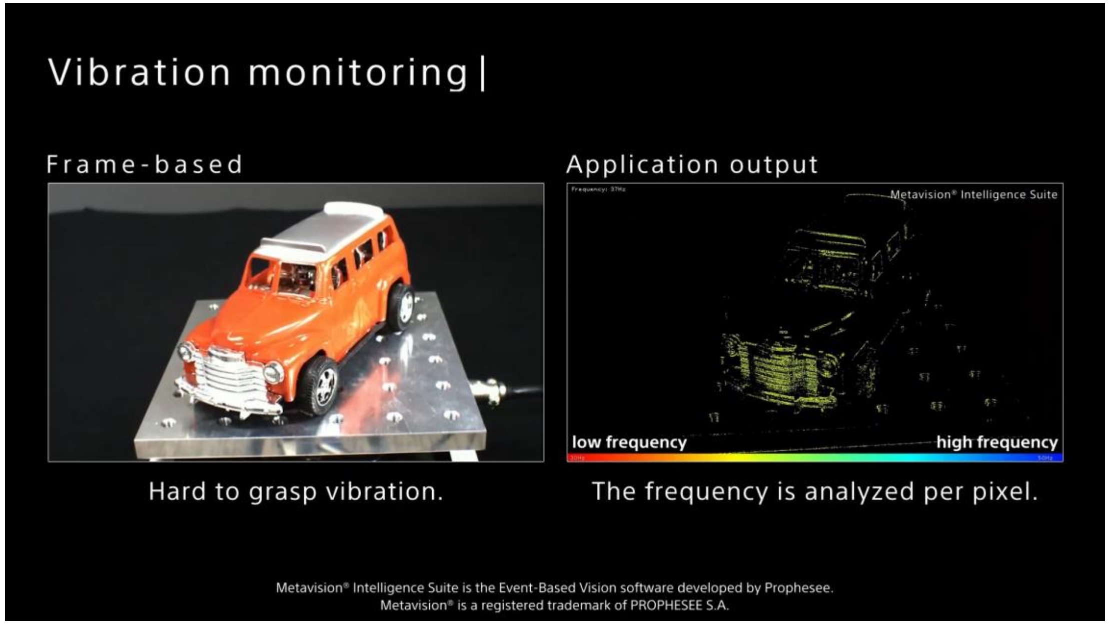
# Demonstration of Application Examples

**Applications utilizing high-temporal-resolution asynchronous event detection are being explored for industrial equipment applications.**




Metavision® Intelligence Suite is the Event-Based Vision software developed by Prophesee.
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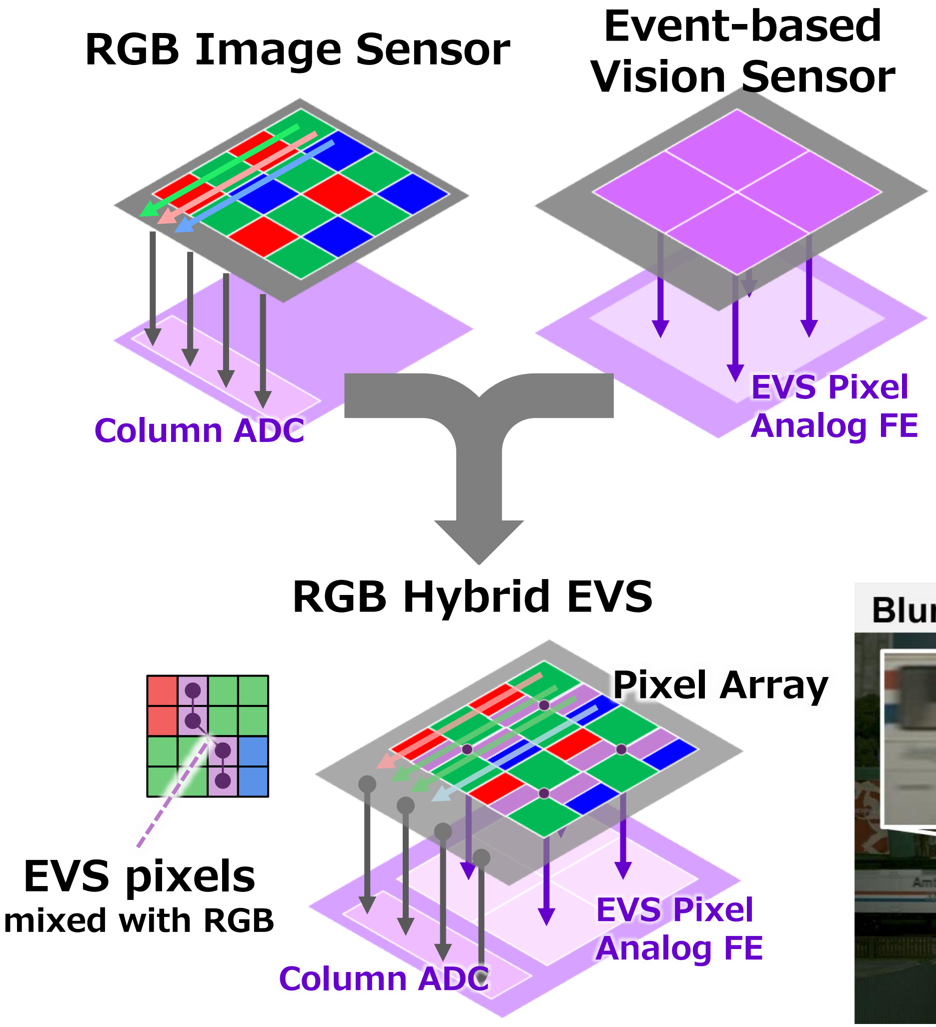
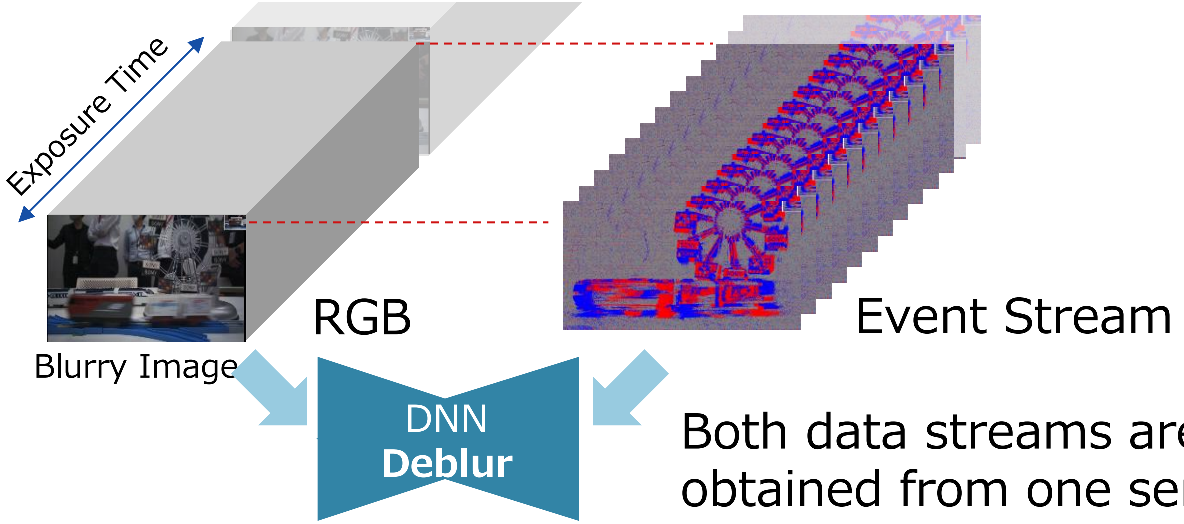
# Integration of Sensing Capability into Imaging Applications

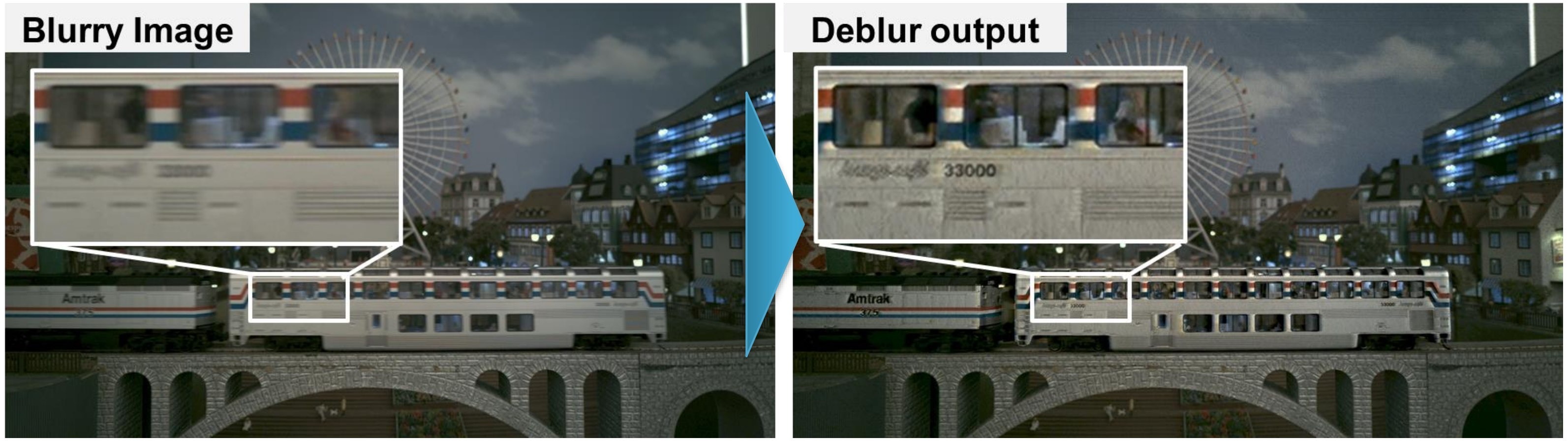
## Combining RGB and EVS for image enhancement through DNN.




Both data streams are obtained from one sensor

K. Kodama, ISSCC2023



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# Integration of Sensing Capability into Imaging Applications

**Event Stream can help very smooth video frame interpolation.**

**15 frames per second by Conventional Color Sensor**



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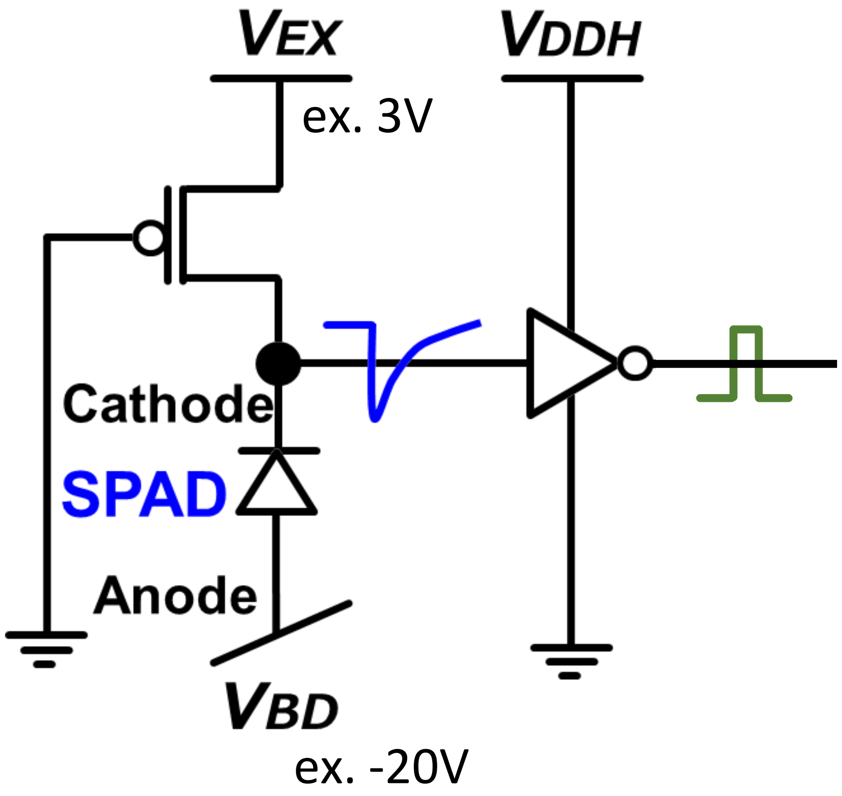
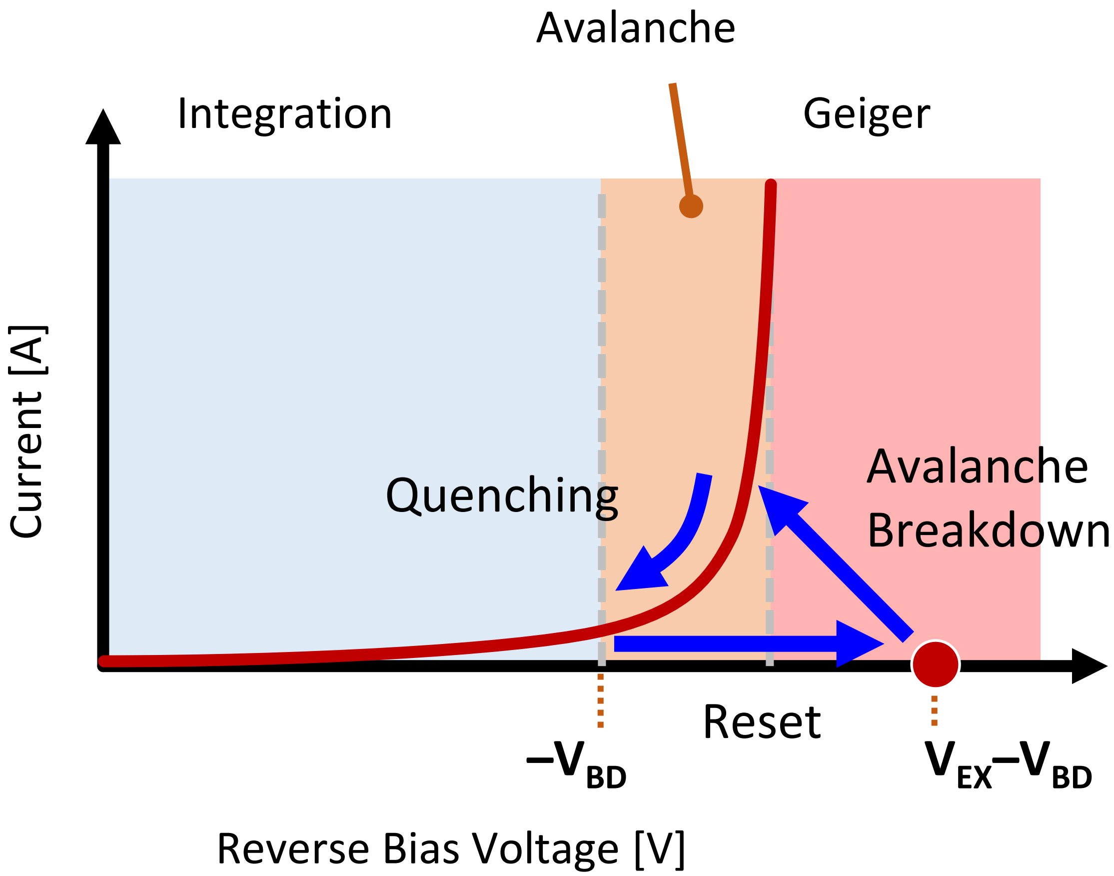
# Single Photon Avalanche Diode (SPAD)

**Avalanche breakdown is triggered by an incident photon, then a quenching register drops the bias to stop the avalanche.**





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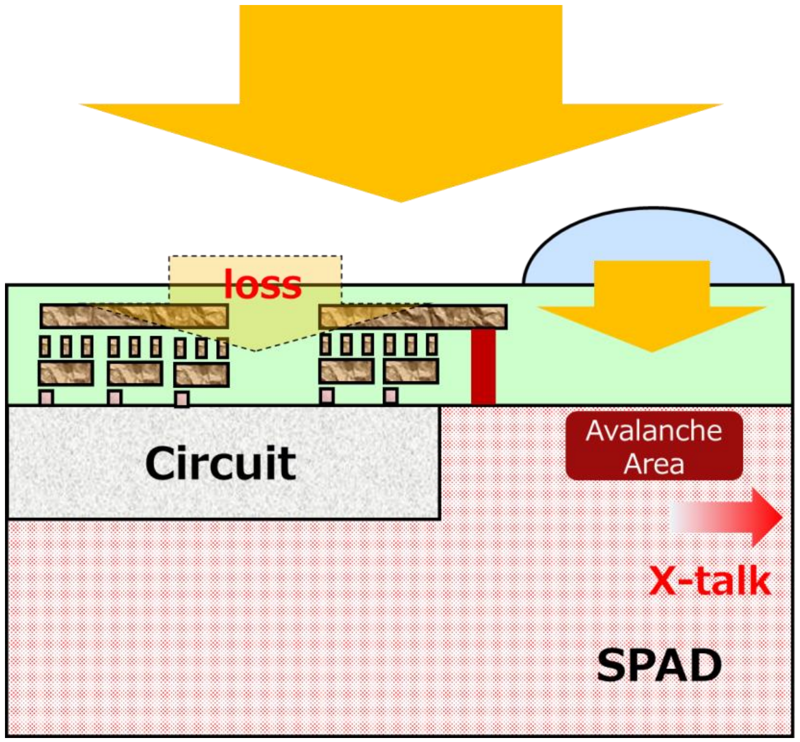
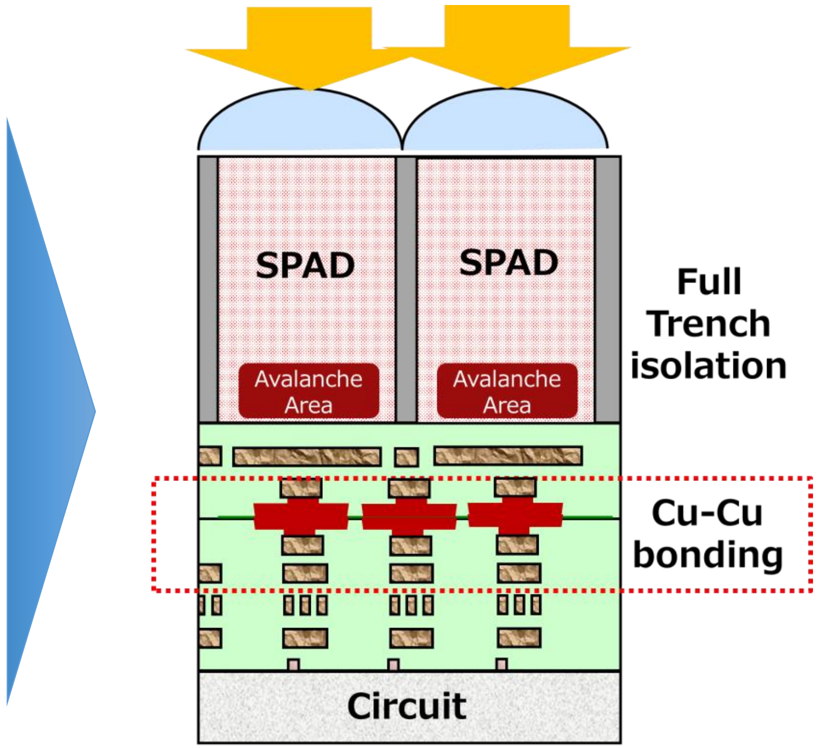
# SPAD Pixel Evolving with Cu-Cu Connections

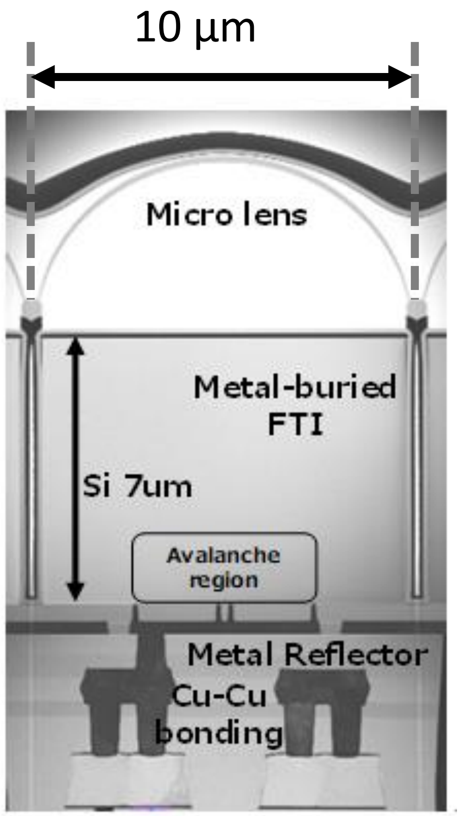
**Stacked device technology is a promising breakthrough of SPAD.**

## Conventional SPAD Pixel




## State-of-the-art SPAD Pixel




K. Ito, IEDM 2020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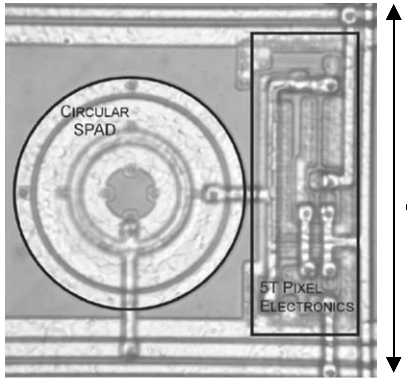
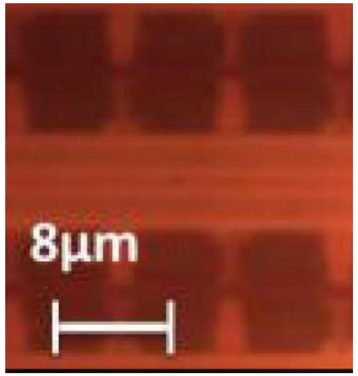
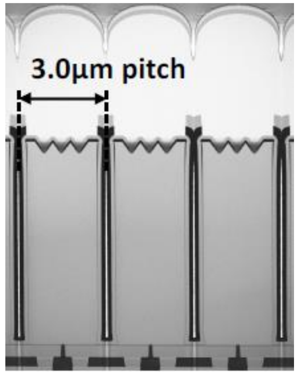
# SPAD Technology Evolution

| The origins | FSI Optimized | BSI Optimized |
|---|---|---|
|   58mm |   8mm |   3mm |
| *C. Niclass, JSSC 2005* | *N. Dutton, TED 2016* | *S. Shimada, IEDM 2022* |
| Tech.: 0.8mm FSI | Tech.: 130nm FSI | Tech.: 90nm BSI, stacked |
| Fill Factor: 1.1% | Fill Factor: 26.8% | Fill Factor: 100% |
| DCR=350Hz@RT | DCR~50Hz@RT | DCR~2Hz@RT |
| PDE~0.29% | PDE~10% | Peak PDE~78%@Vex=3.0V |
| NEP=3.5E-15 [W·Hz$^{-0.5}$] | NEP=4.0E-17 [W·Hz$^{-0.5}$] | NEP=1.0E-18 [W·Hz$^{-0.5}$] |

**In less than 20 years: Pixel pitch shrunk x20, NEP improved x$10^3$**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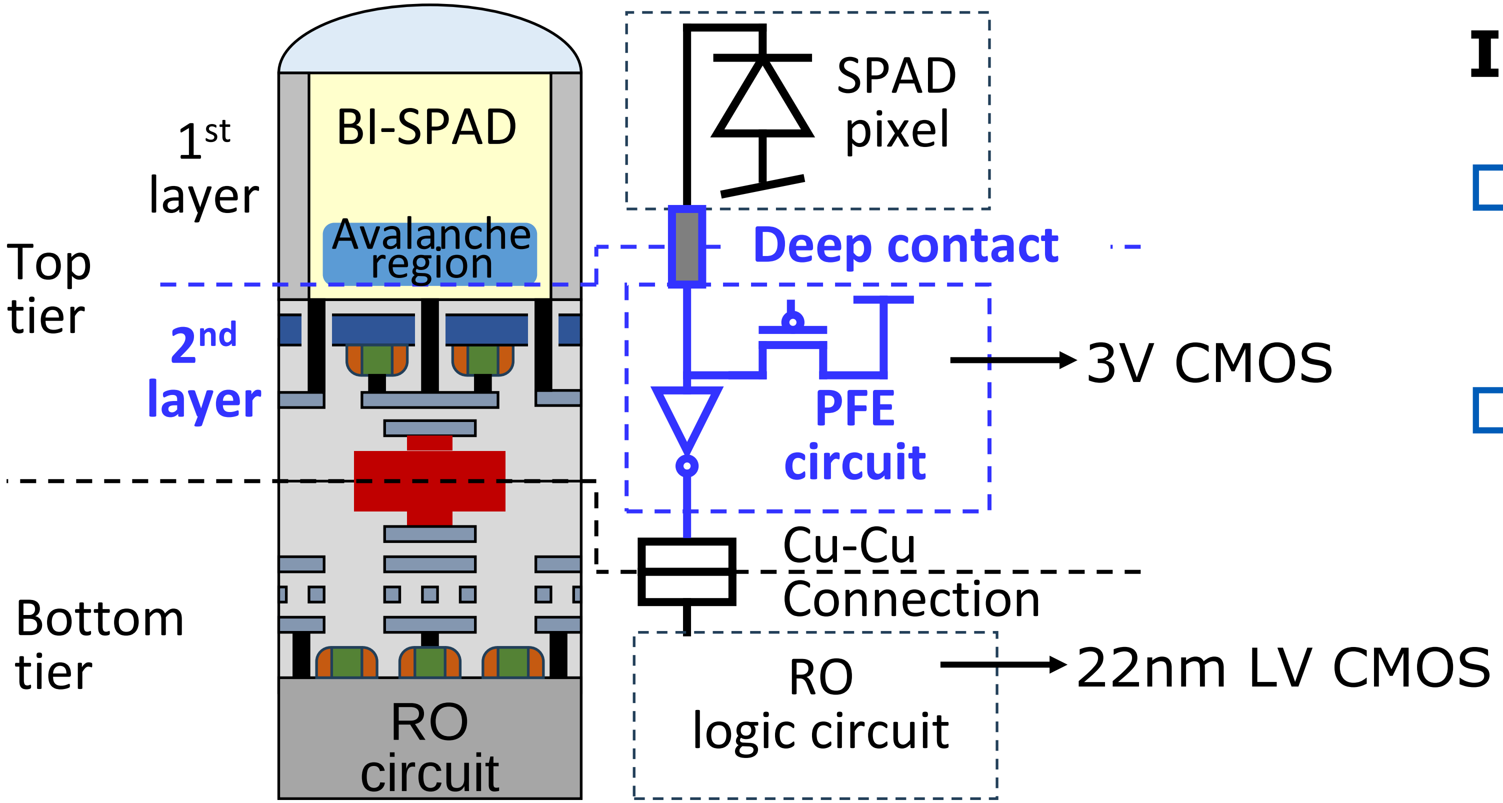
# SPAD Evolution : 3D Stacked 2-layer CMOS




*J. Ogi et al., IEDM'24*

**Innovation drivers**:

- 3rd level stacking increases area for pixel-level logic (+40%)
- Deep contact enables reduction of cathode capacitance (x0.5)
  - Avalanche current ~60% lower
  - Dead time 1/3rd

→ Superior performance at high photon-flux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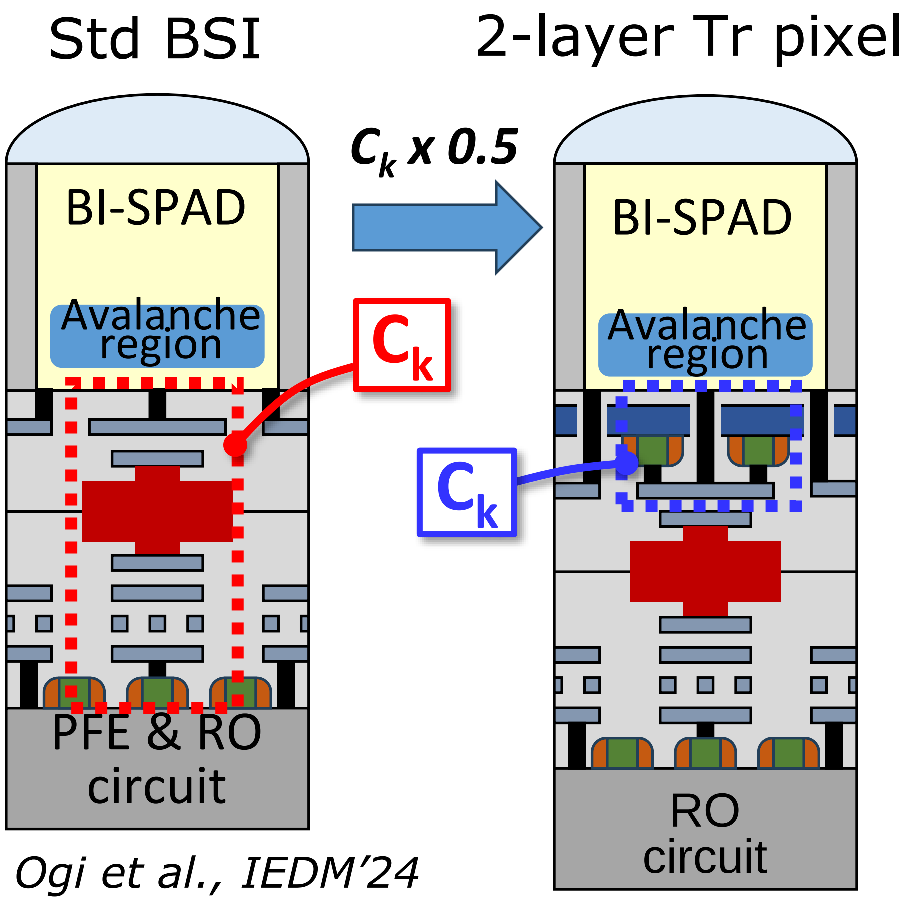
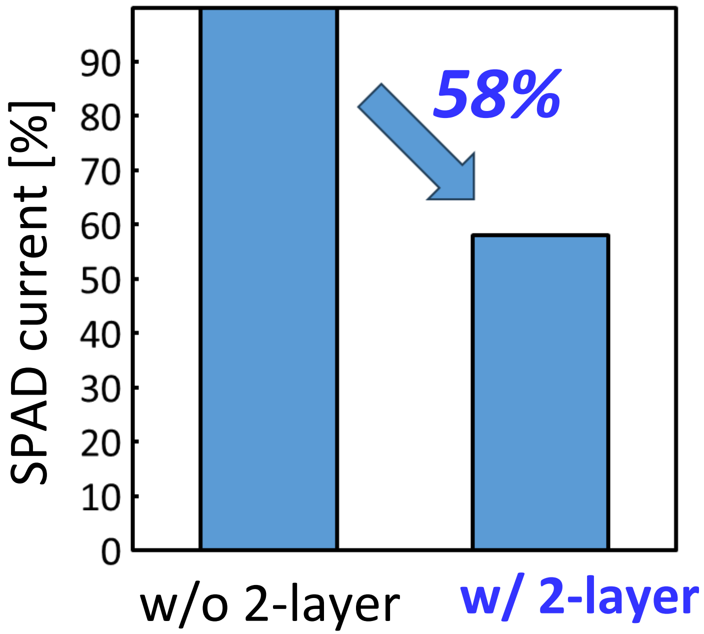
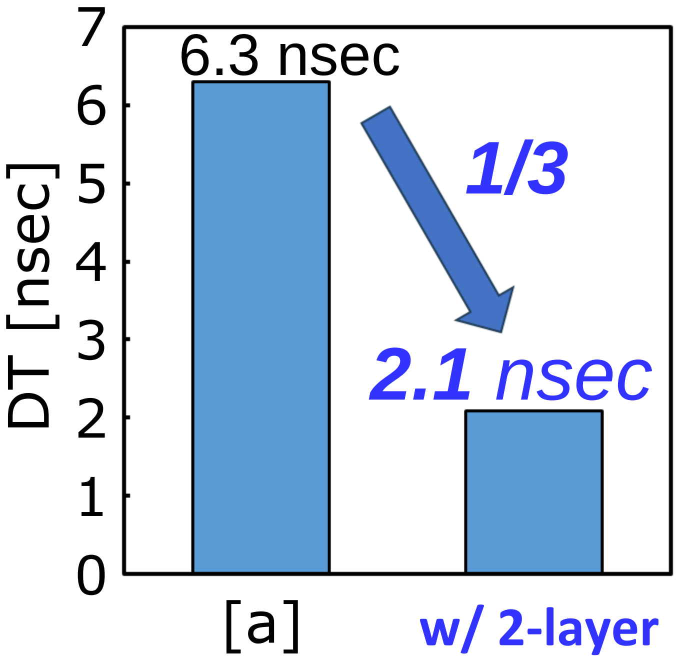
# SPAD Evolution : Reducing Avalanche charge




J. Ogi et al., IEDM'24




[a] S. Shimada et al., IEDM'21

- SPAD cathode capacitance reduced to half: reducing SPAD current by 58% and deadtime to 1/3$^{rd}$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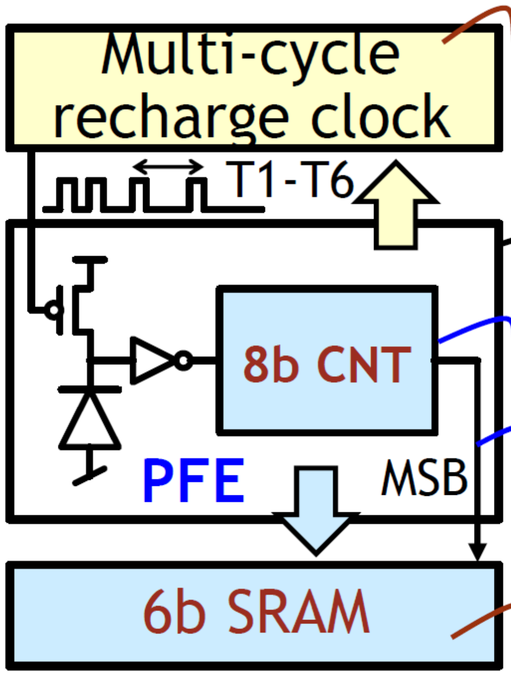
# SPAD Evolution : In-pixel SPAD FE & counter within each pixel

This work




Clustered multi-cycle clocked recharging (CMCR) for HDR

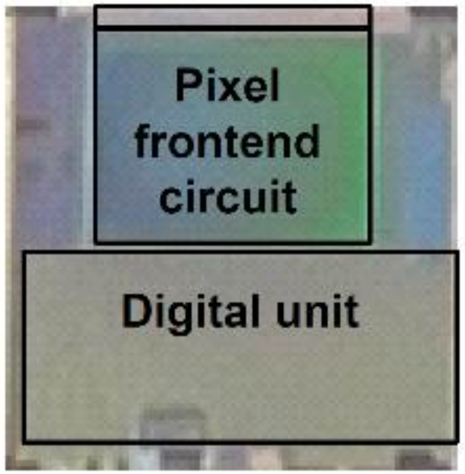

3.36 µm-pitch

Simple 8-bit counter for small pixel size

Overflow counting during exposure for sufficient SNR

Upper count bits

Bottom-tier (Logic 22 nm)




- 8-b counter within each pixel, MSBs moved outside pixel array

[T. Takatsuka, VLSI 2023]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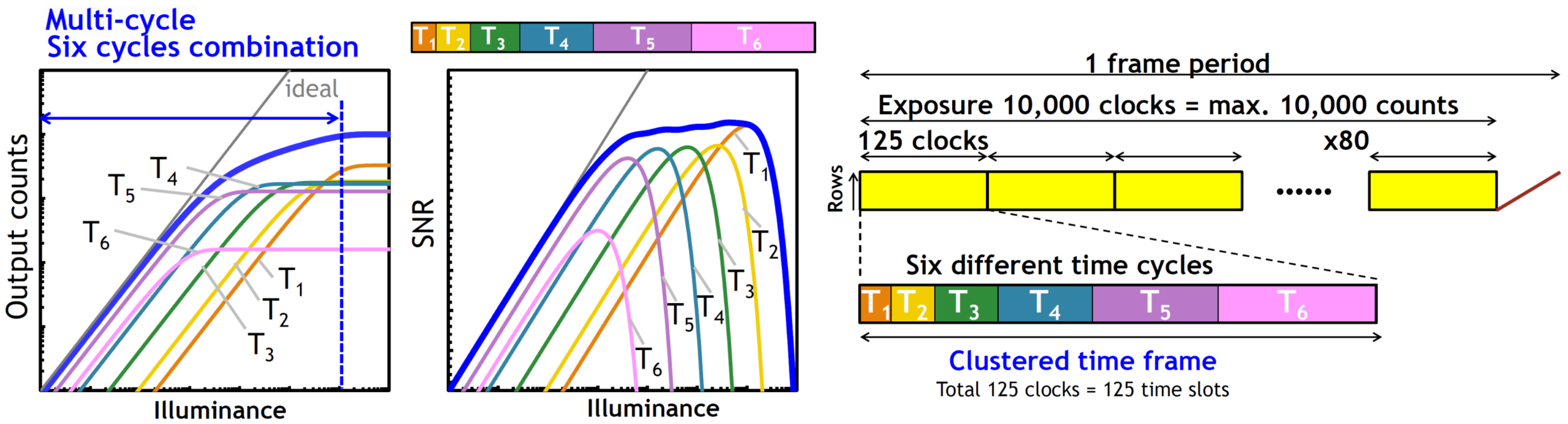
# SPAD Evolution : HDR

## HDR without SNR dip achieved by Multi-Cycled Clocked Recharging




[T. Takatsuka, VLSI 2023]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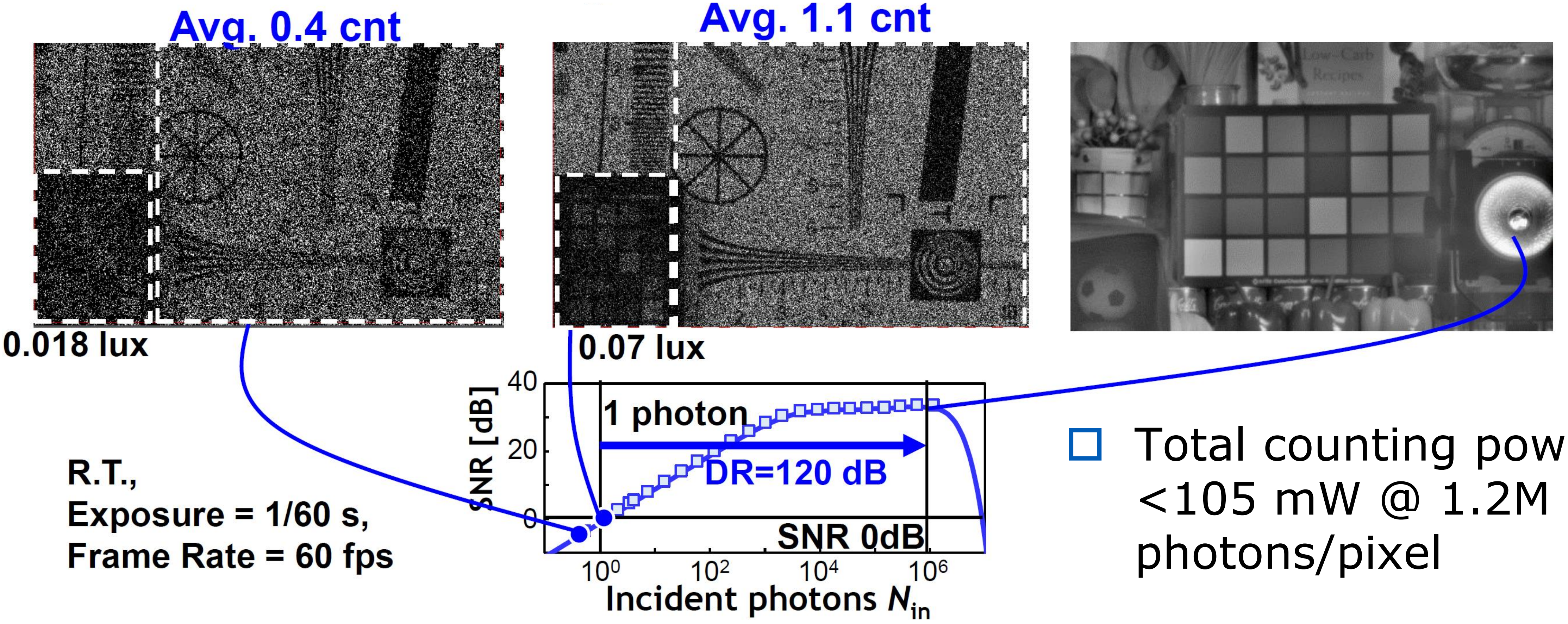
# SPAD Evolution

**Demonstrated imaging with <1 to 1M photons, 120dB DR**




- Total counting power <105 mW @ 1.2M photons/pixel

[T. Takatsuka, VLSI 2023]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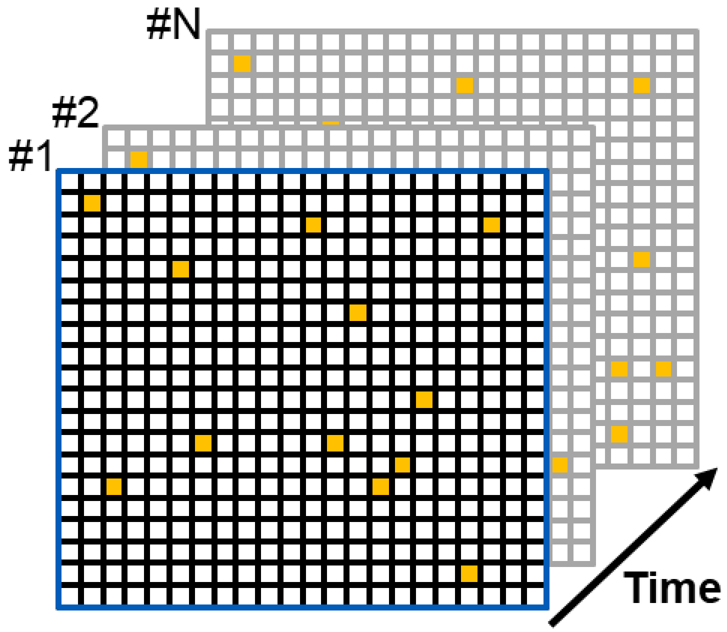
# Quanta Image Sensor (QIS)

- QIS = photon-counting image sensor
- Early concept of QIS back to ‘60s (PMT), later with APDs ‘80s
- QIS paradigm postulated by E. Fossum[1]:
  - Detect each photo-electron
  - Create sparse, binary bit-planes at high frame rates
- Two families of QIS:
  - SPAD
  - High conversion gain / sub-$e^-$ input-referred noise PPD
- Digital Photon Counting Imagers = dPCT CIS
- dPCT is a class of QIS: pixel-level multibit digital photon counting




*[1] E. Fossum, IEEE Workshop on CCD and Advanced Image Sensors, 2005*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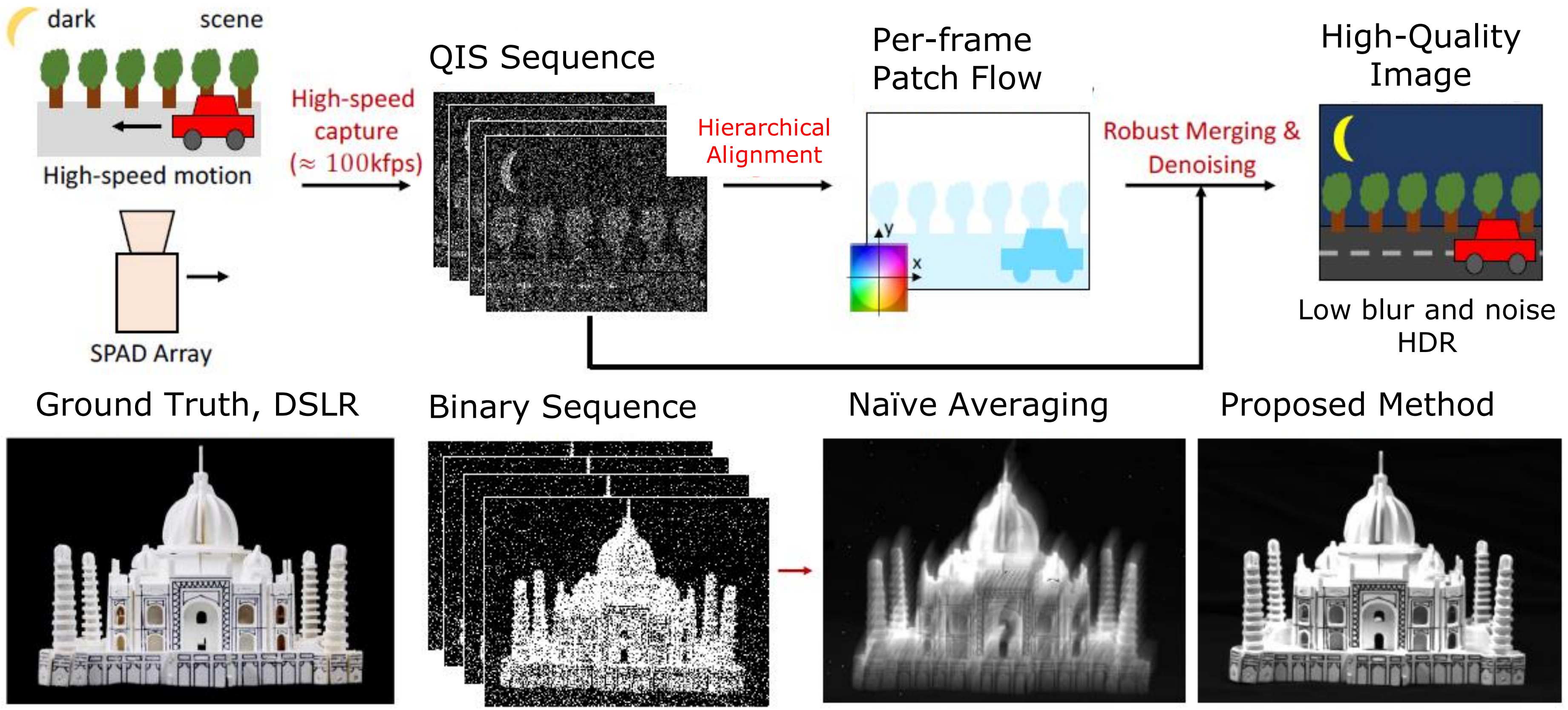
# Quanta Burst Photography: the 'Magic' of QIS

- QIS capture high speed stochastic images very close to physical limit
- Clever post-processing allows recovering SNR with marginal motion blur




*S. Ma et al, ACM Trans. Graph., 2020*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